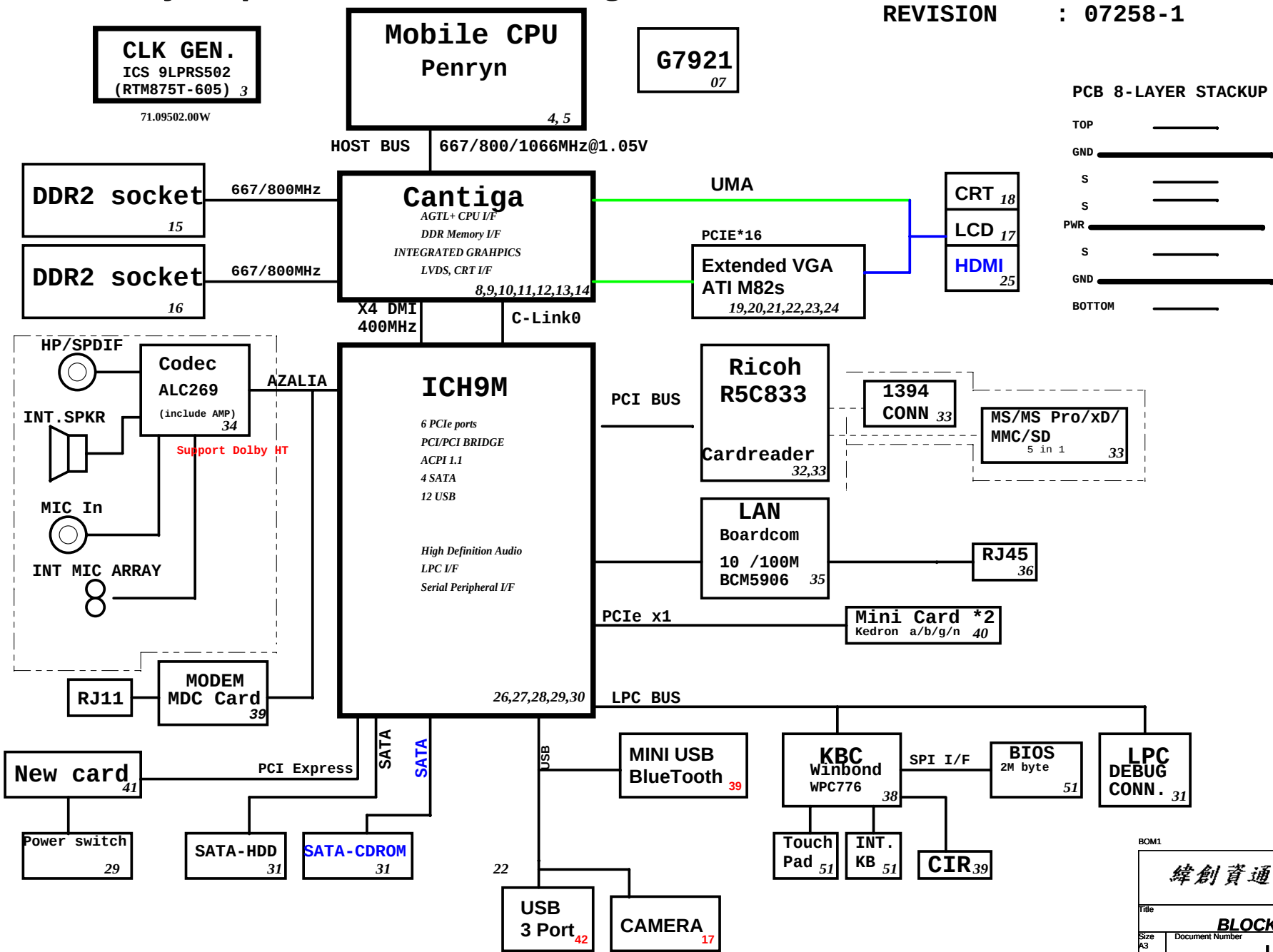


Olympus Block Diagram

Project code: 91.4Y601.001
PCB P/N : 48.4Y603.0SA
REVISION : 07258-1



SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5A) 3D3V_S5 (5A)
SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M (11A) 1D5V_S3 (10A)
TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5308 39	
3D3V_S0	2D5V_S0 (300mA)
CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
SC411 48	
DCBATOUT	1D5V_S3

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BLOCK DIAGRAM	
Size A3	Document Number LT32M
Date: Tuesday, May 13, 2008	Rev -1
Sheet 1	of 55

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers: Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers: Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT14#/GPIO51	ESi Strap (Server Only) Rising Edge of PWROK	ESi compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PC1, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

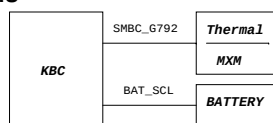
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1667 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG6 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 01 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital Display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
LDDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

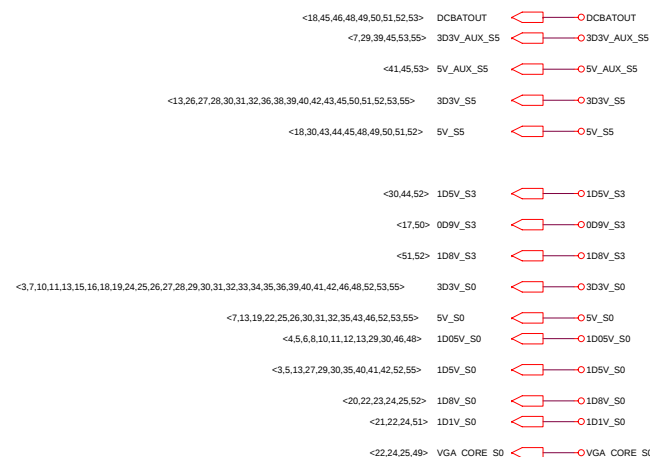
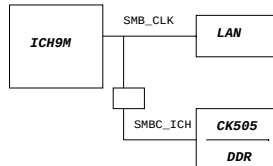
PCI Routing

page 17

IDSEL	INT	REQ	GNT
TI7412	AD22	6: CARDBUS B: 1394 F: Flash Media G: SD Host	0 0

PCIE Routing

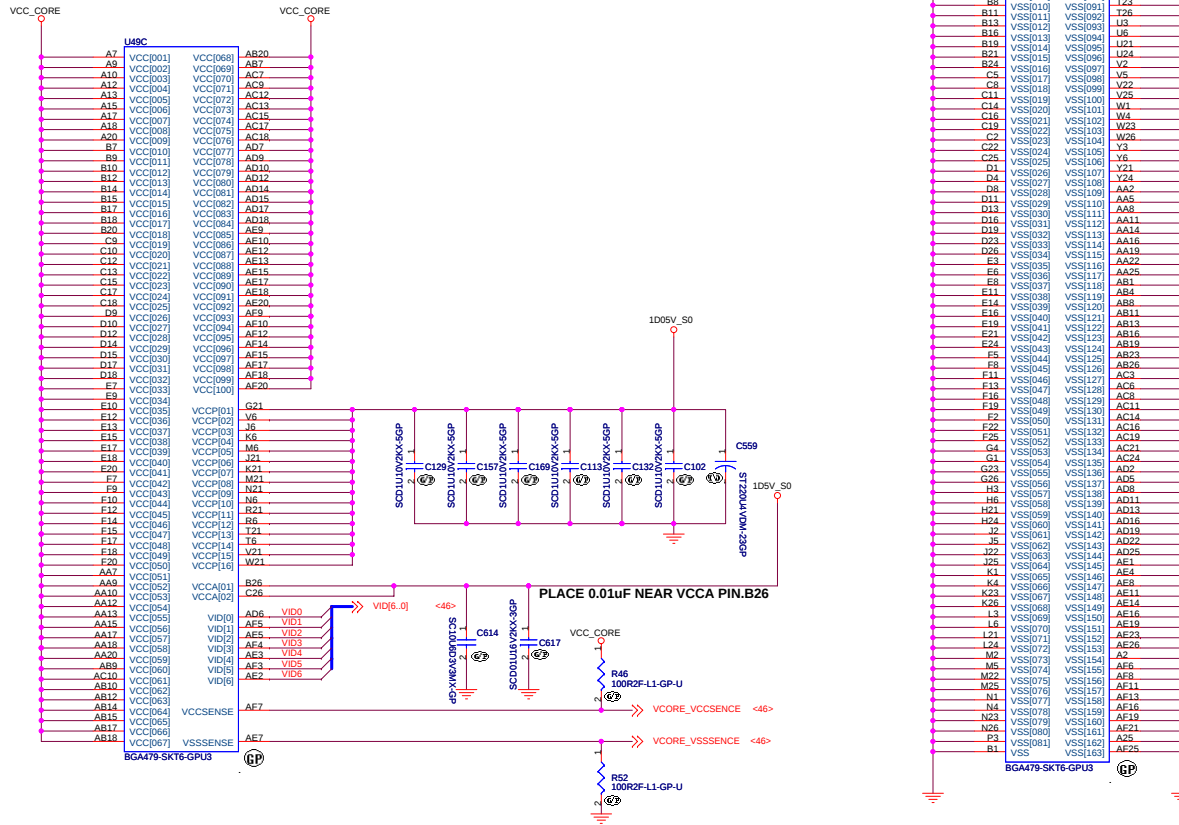
LANE2	MiniCard WLAN
LANE3	NewCard WLAN



ROM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshih,
Taipei Hsien 221, Taiwan, R.O.C.

Reference			
Size C	Document Number	Rev	
	LT32M	-1	
Date: Tuesday, May 13, 2008	Sheet 2	of	54



BOM1

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File

Penryn CPU(2/2)

Size

Document Number

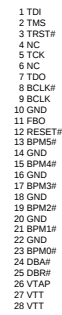
LT32M

Rev

-1

Date: Tuesday, May 13, 2008

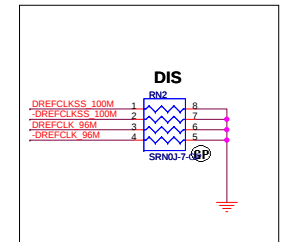
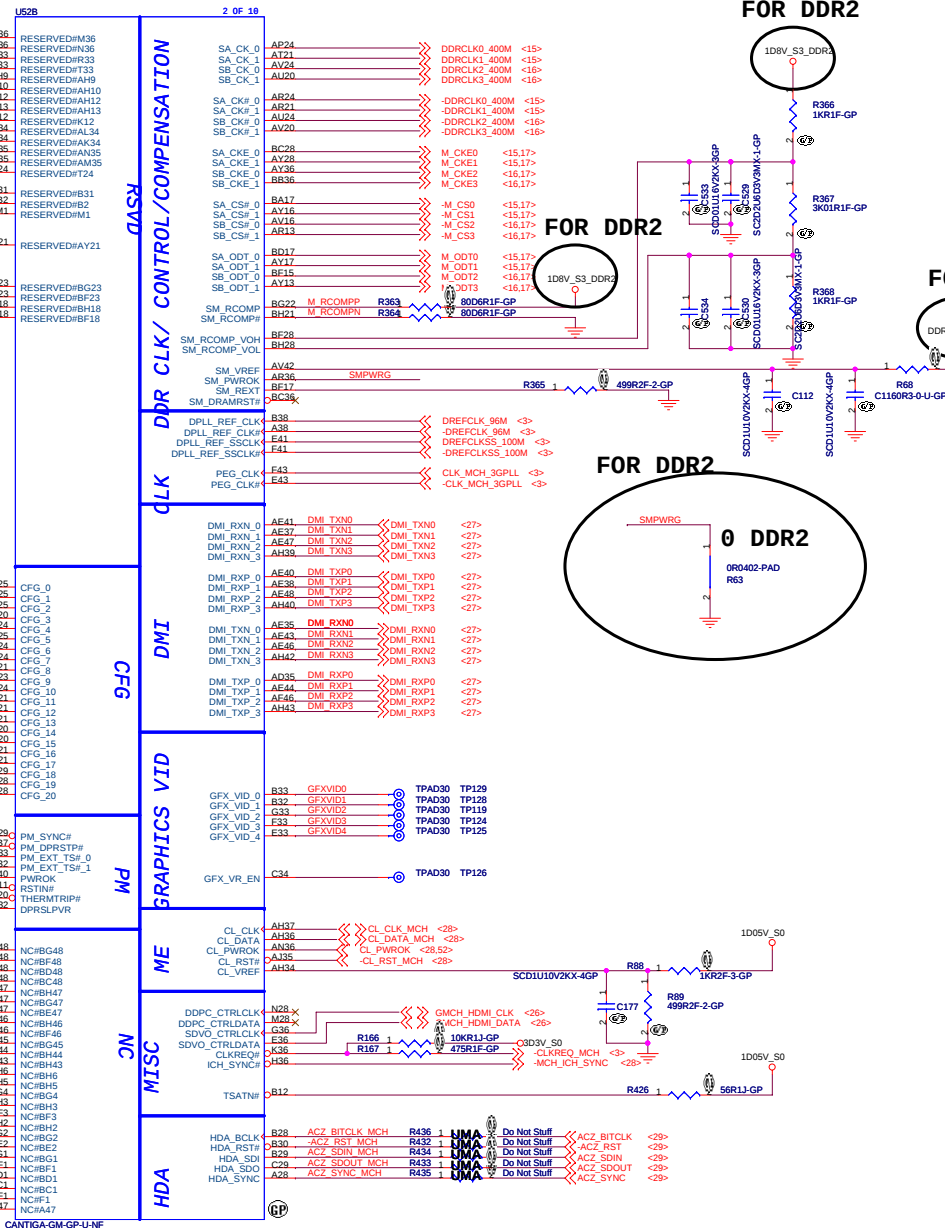
Sheet 5 of 54



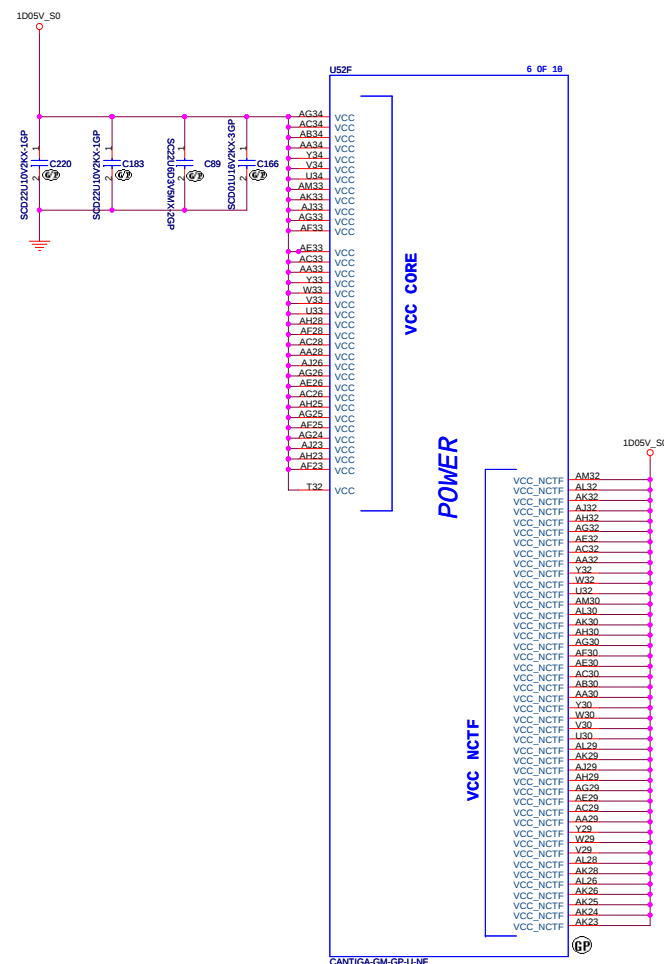
Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% AS
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

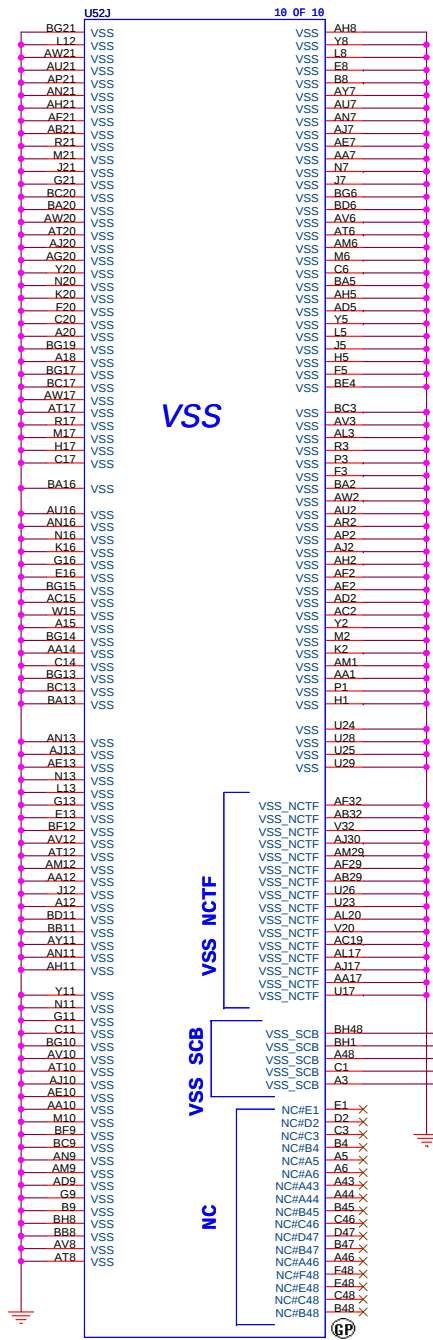
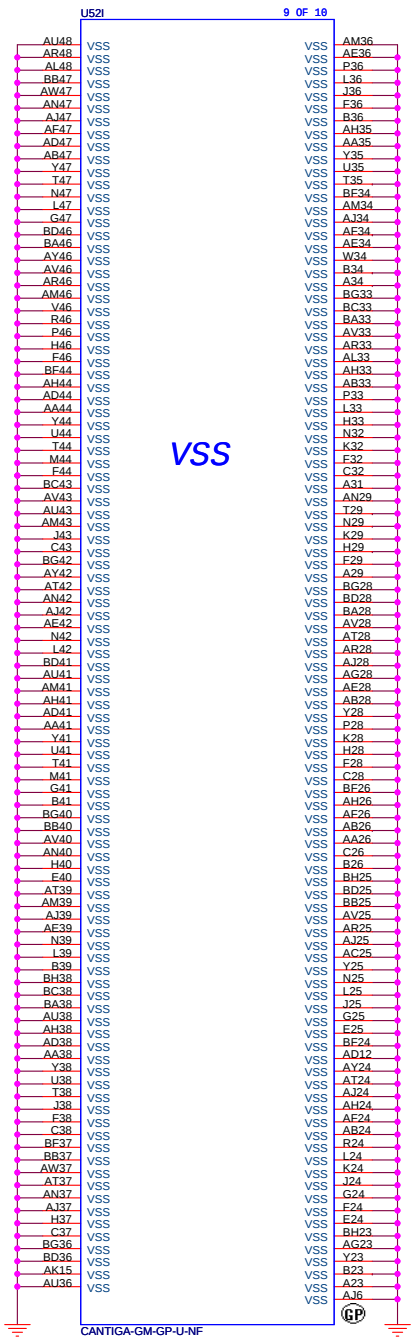


RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

[illegible]

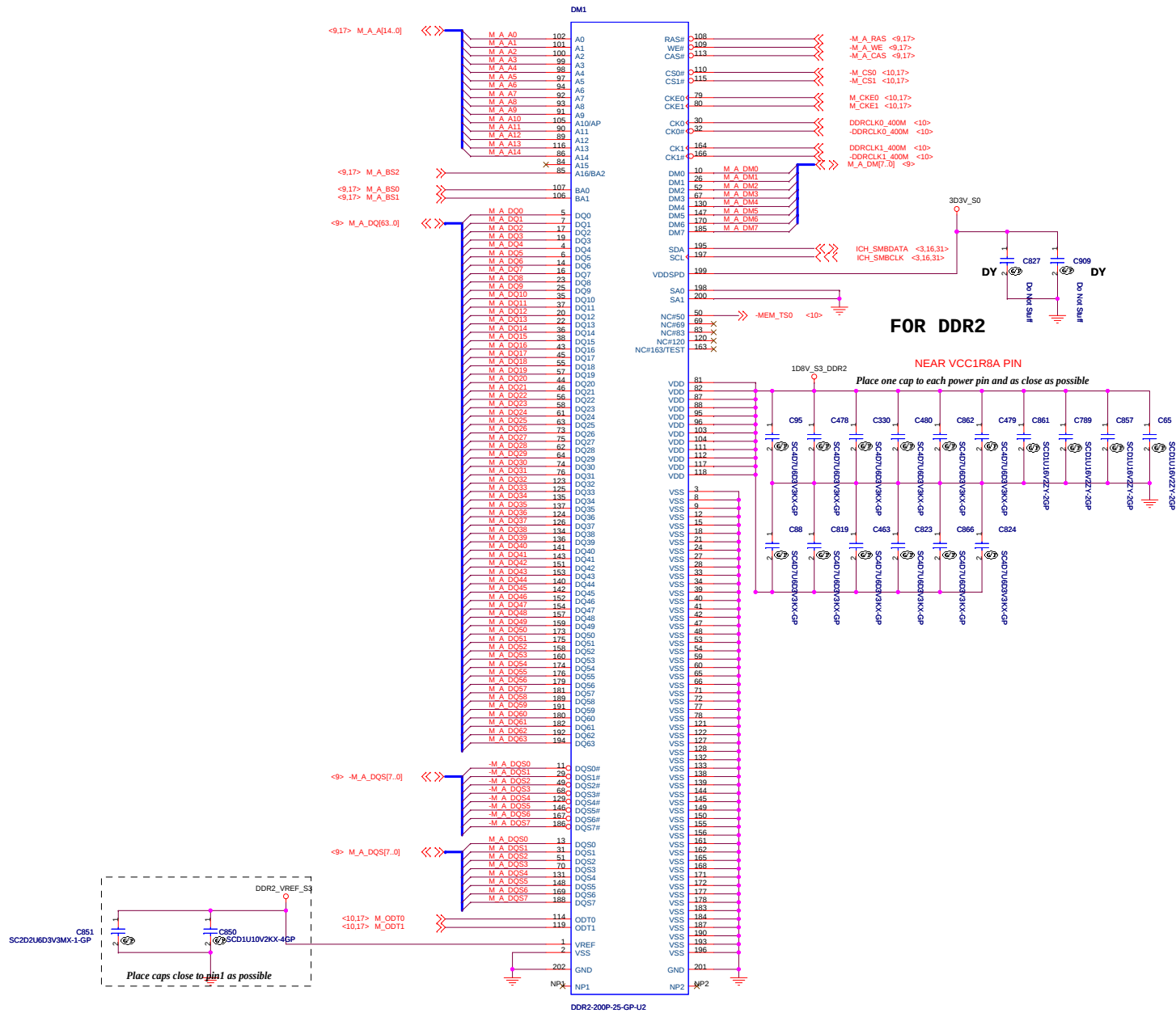
1D8V_S3_DDR2





BOM1

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Title	
Cantiga(8/7): GND	
Size	Document Number
A3	LT32M
Date:	Tuesday, May 13, 2008
Sheet	14 of 54



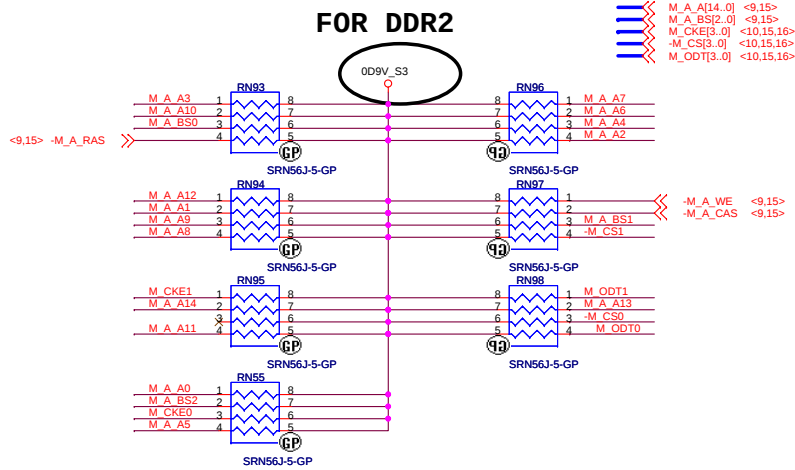
9.2mm High

BOM1

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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DDR2 SODIMM-A			
Size	Document Number		Rev
C	LT32M		-1
Date:	Tuesday, May 13, 2008	Sheet 15 of	54

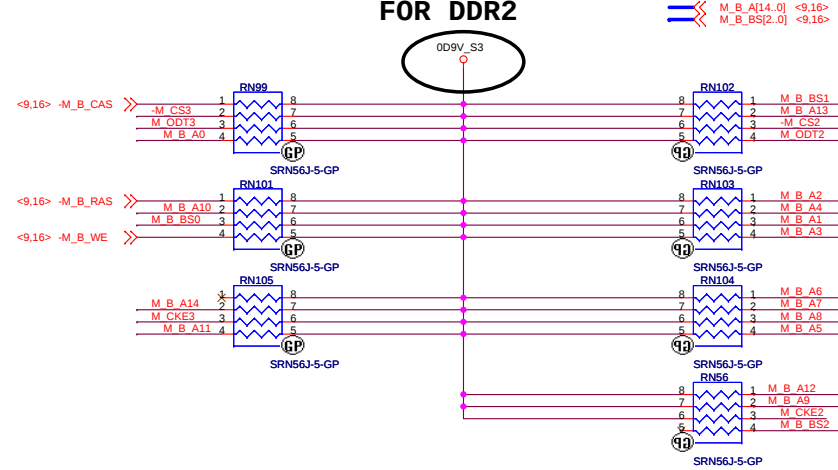
CHANNEL A PARALLEL TERMINATION

FOR DDR2



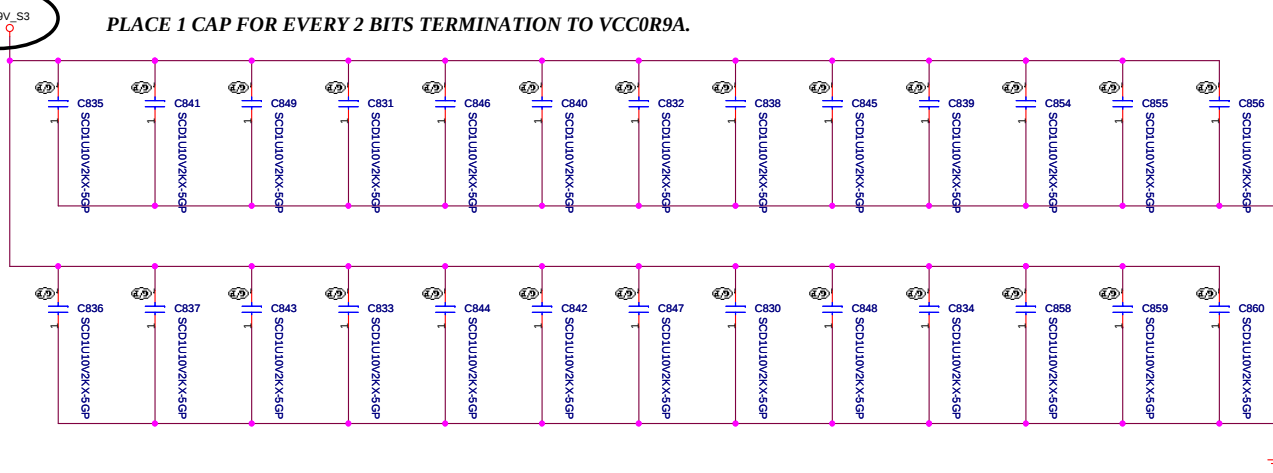
CHANNEL B PARALLEL TERMINATION

FOR DDR2



FOR DDR2

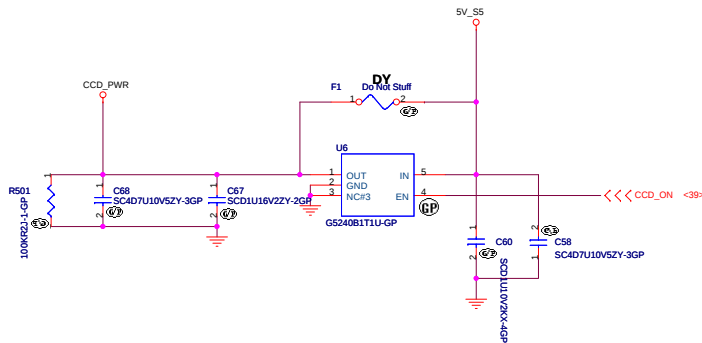
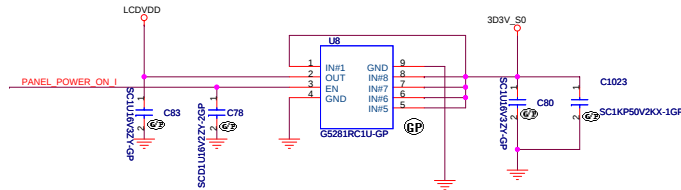
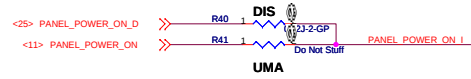
PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO VCC0R9A.



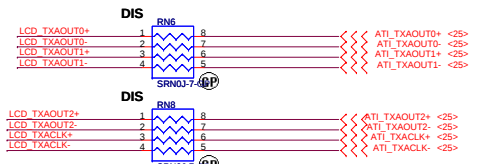
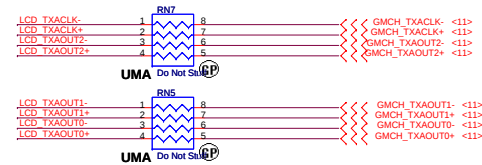
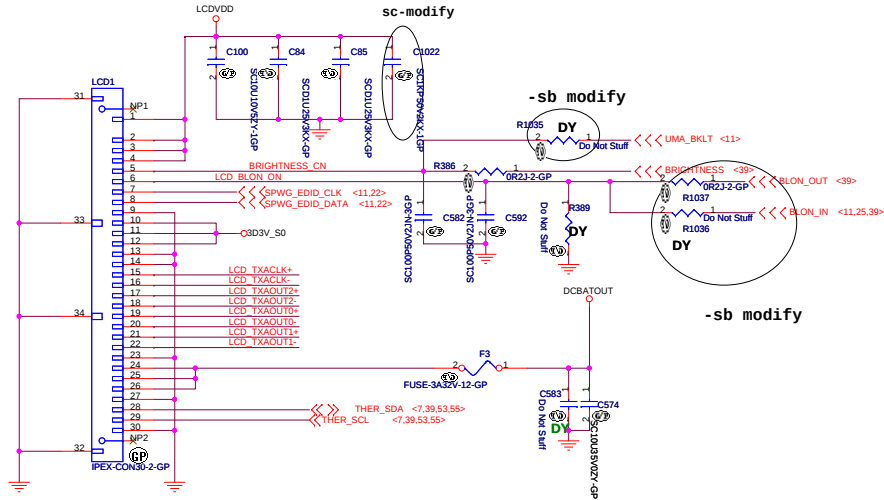
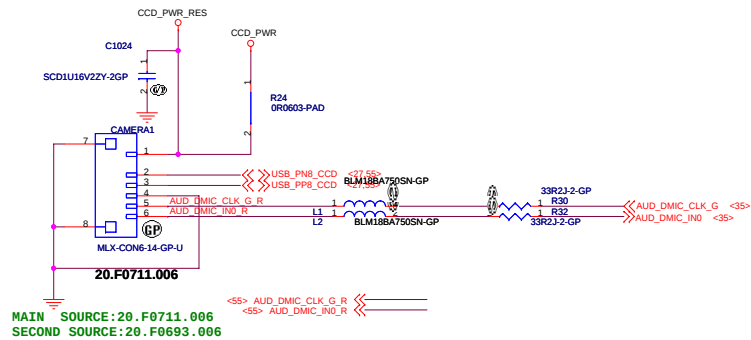
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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DDR-2 TERMINATION/DECOUPLING			
Size	Document Number		Rev
Custom	LT32M		-1
Date: Tuesday, May 13, 2008		Sheet 17 of	54

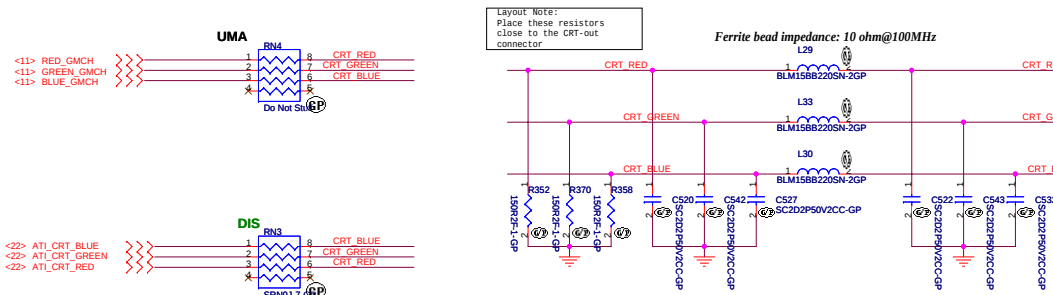
LCD/INVERTER CONN



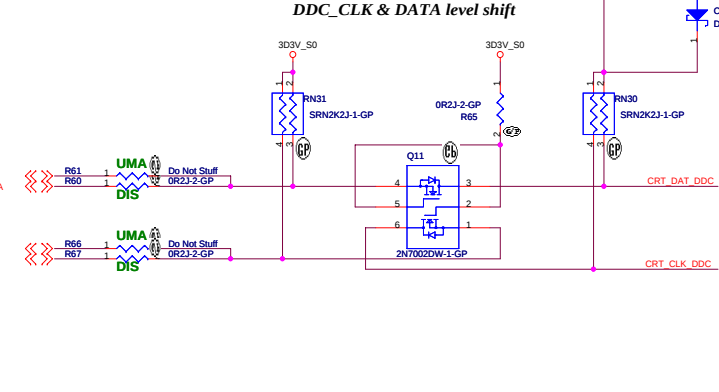
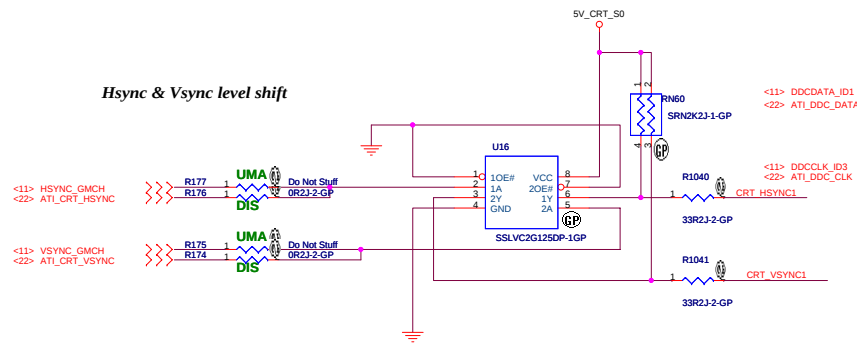
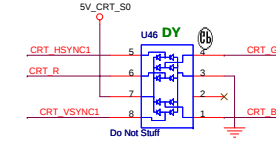
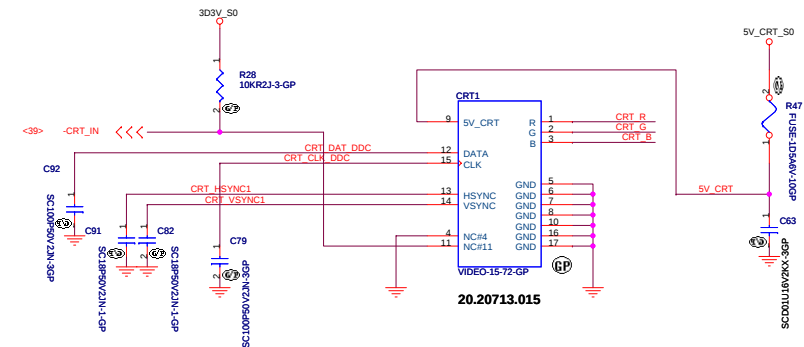
CAMERA & DIG-MIC

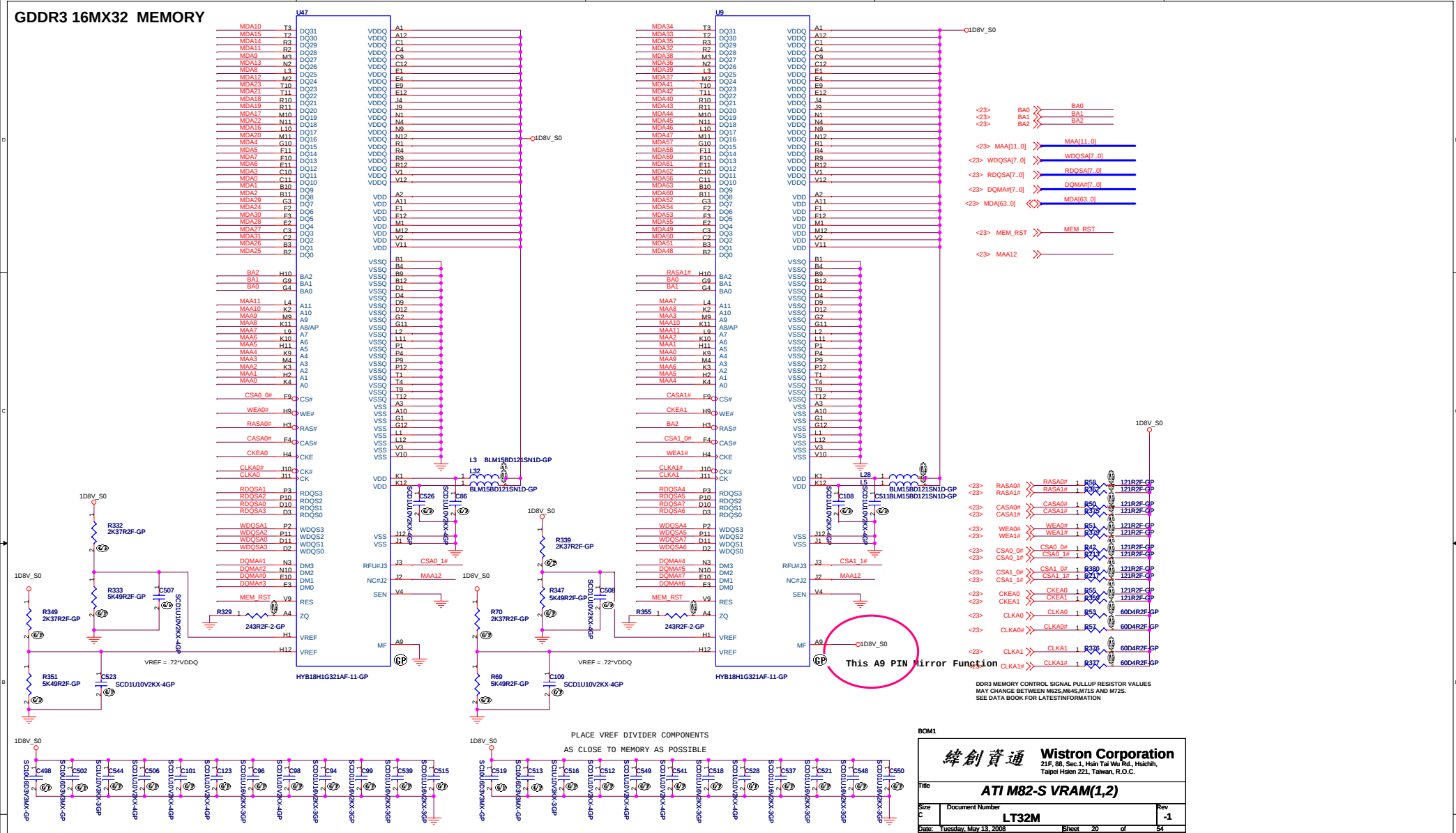


CRT I/F & CONNECTOR

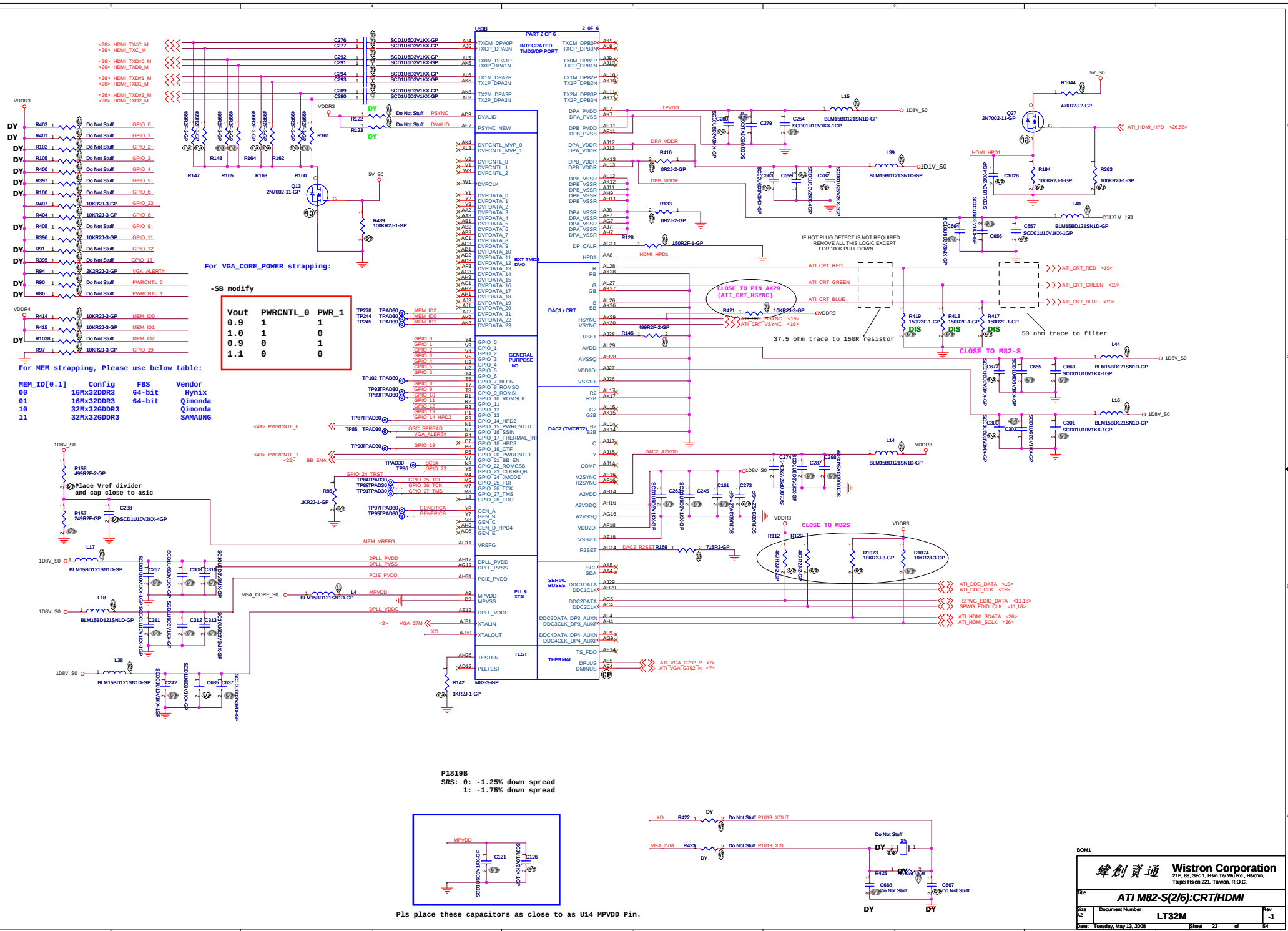


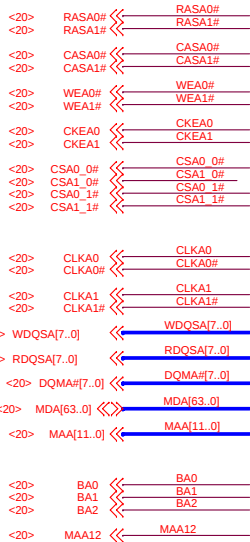
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



GDDR3 16MX32 MEMORY

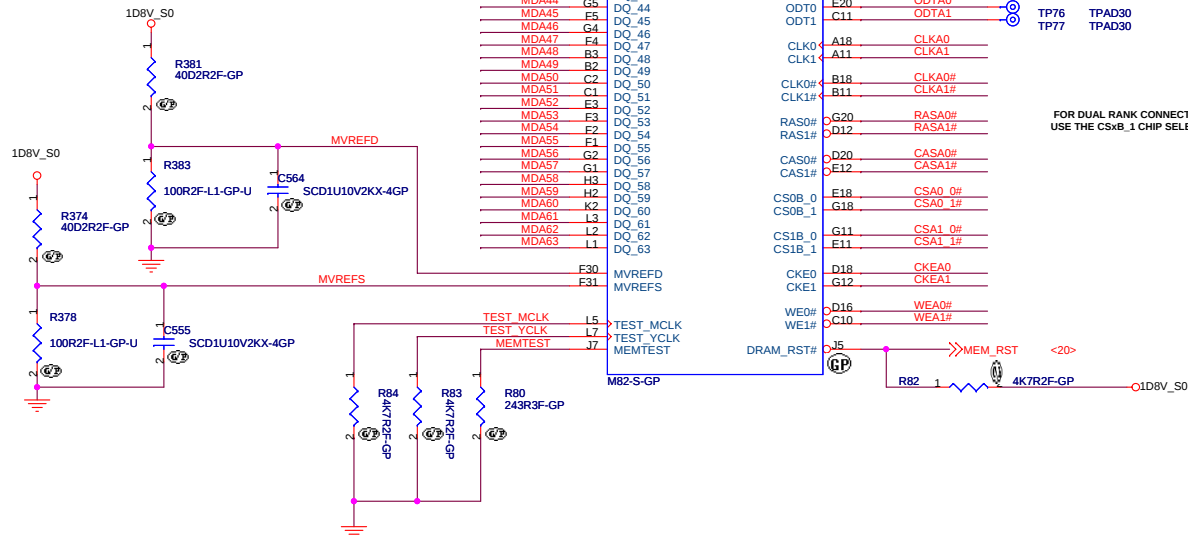
DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M62S,M64S,M71S AND M72S.
SEE DATA BOOK FOR LATEST INFORMATION





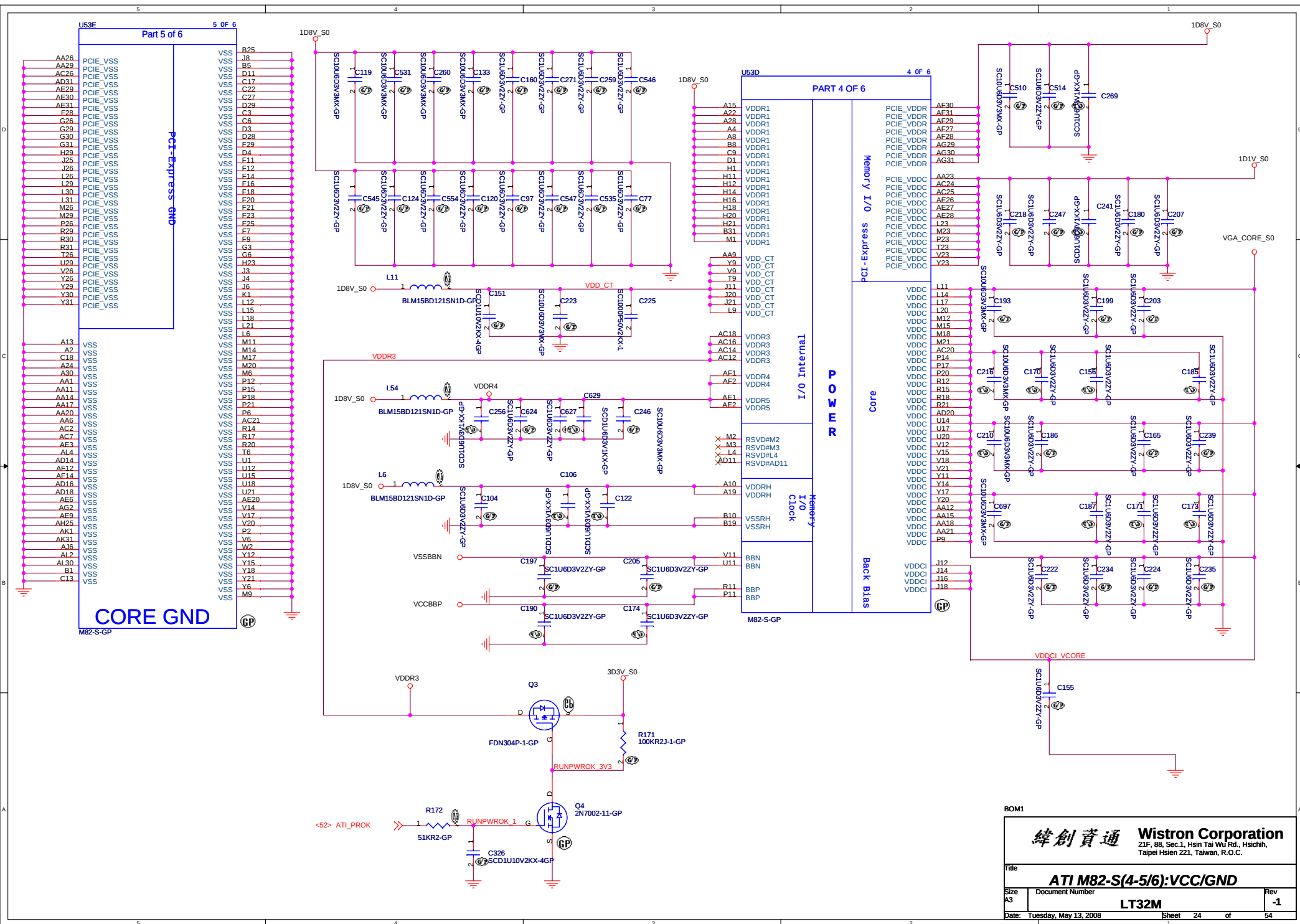
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

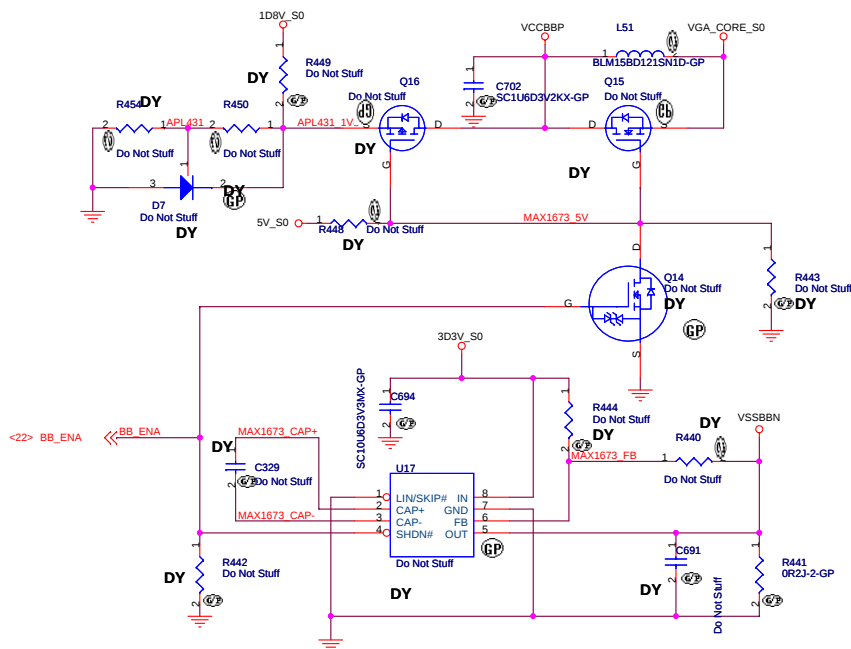
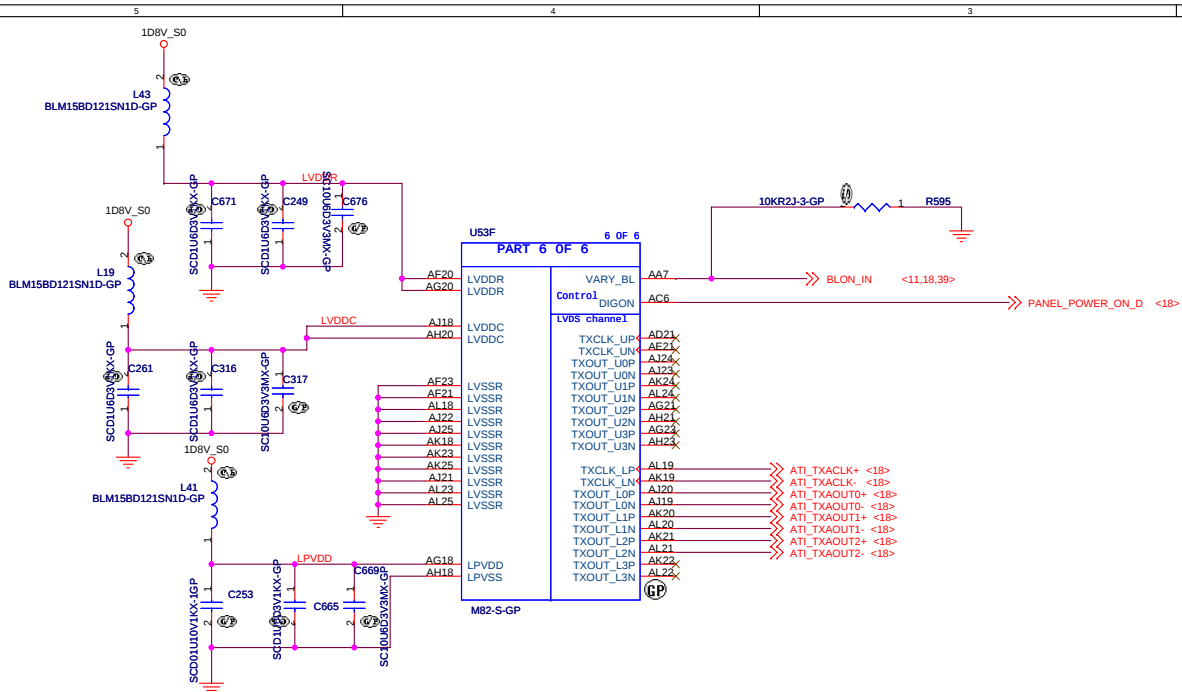
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



BOM1

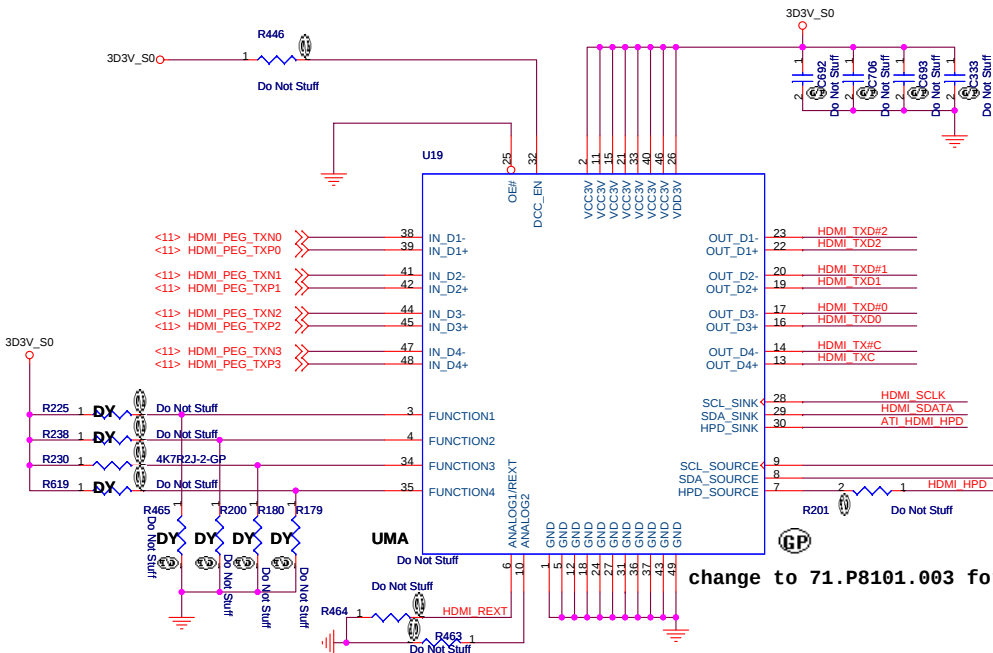
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Title ATI M82-S(3/6):Memory Interface	
Size A3	Document Number LT32M
Date: Tuesday, May 13, 2008	Sheet 23 of 54





BOM1

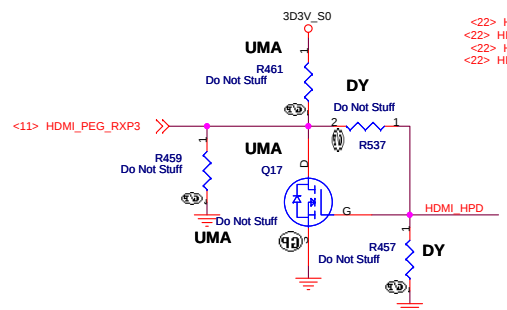
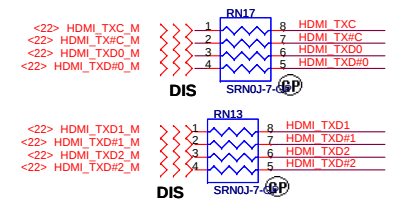
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ATI M82-S(6/6):LVDS		
Title Size Custom	Document Number LT32M	Rev -1
Date: Tuesday, May 13, 2008	Sheet 25 of 54	



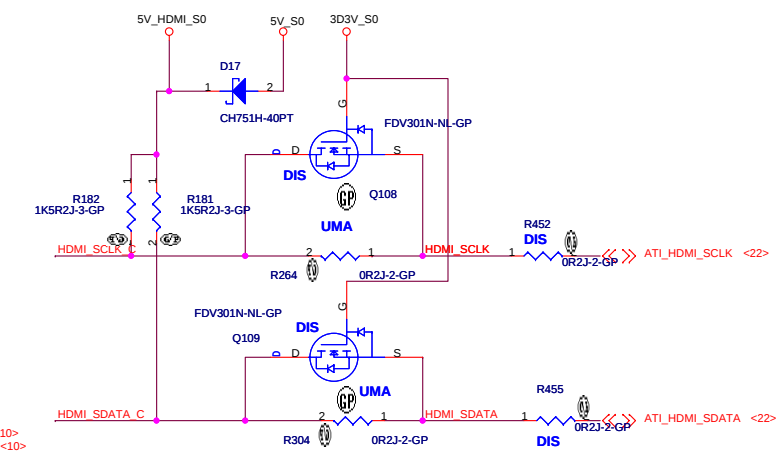
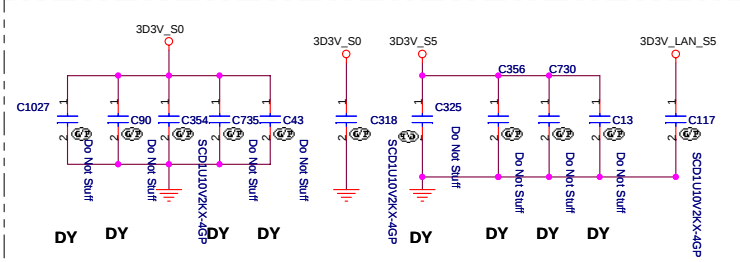
change to 71.P8101.003 for -1

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

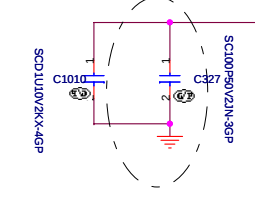
Discrete ASM



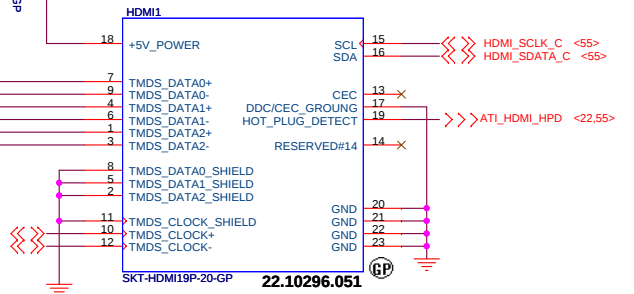
EMI SOLUTION



EMI SOLUTION



HDMI CONN



BOM1

緯創資通

Wistron Corporation

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Title

HDMI CONN

Size

A3

Document Number

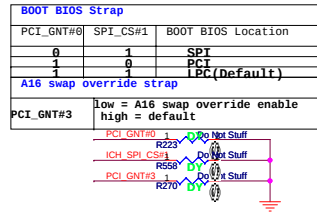
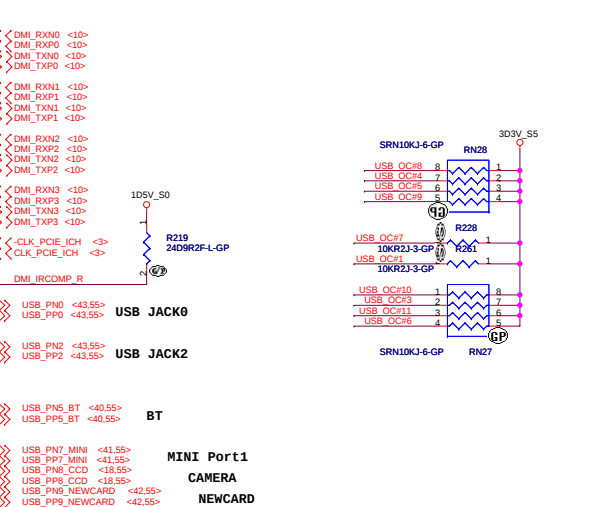
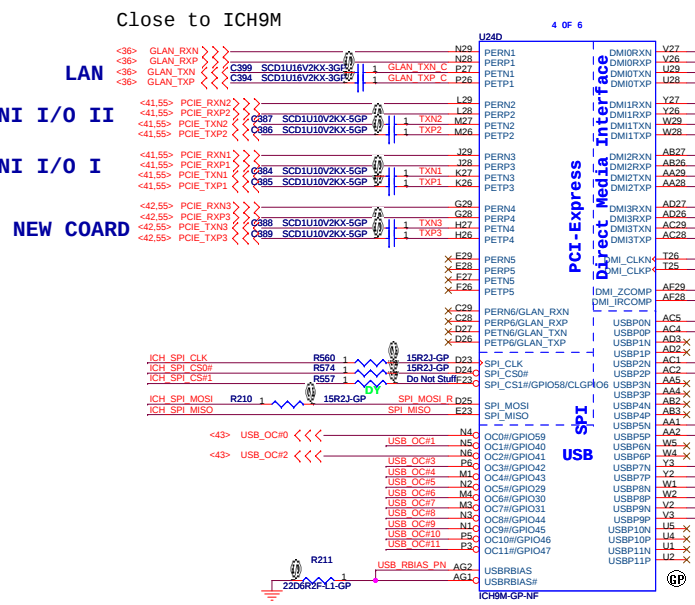
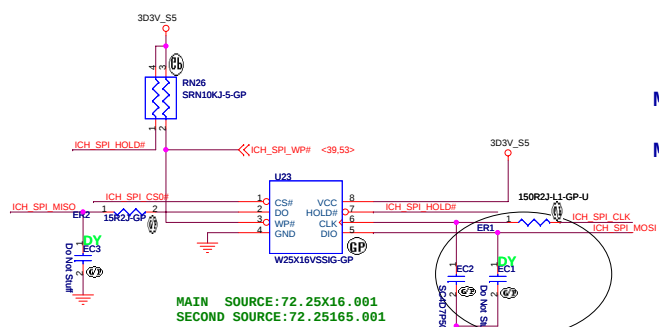
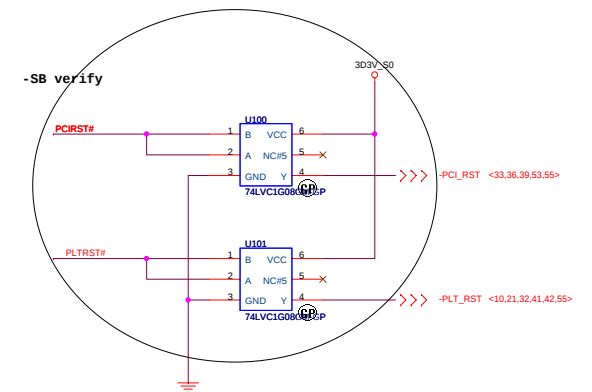
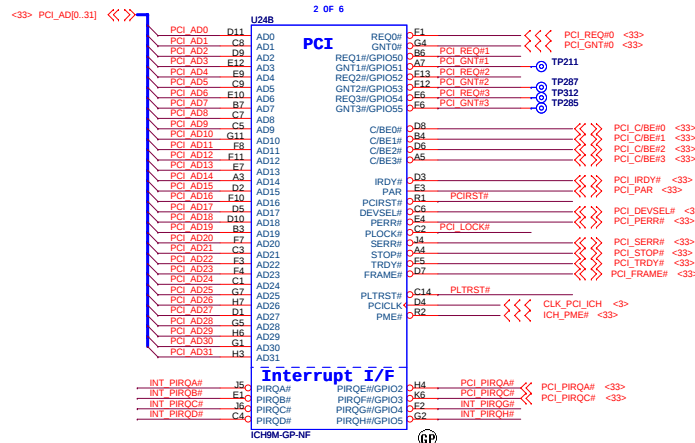
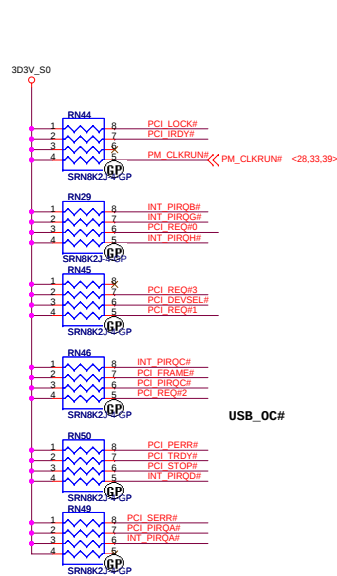
LT32M

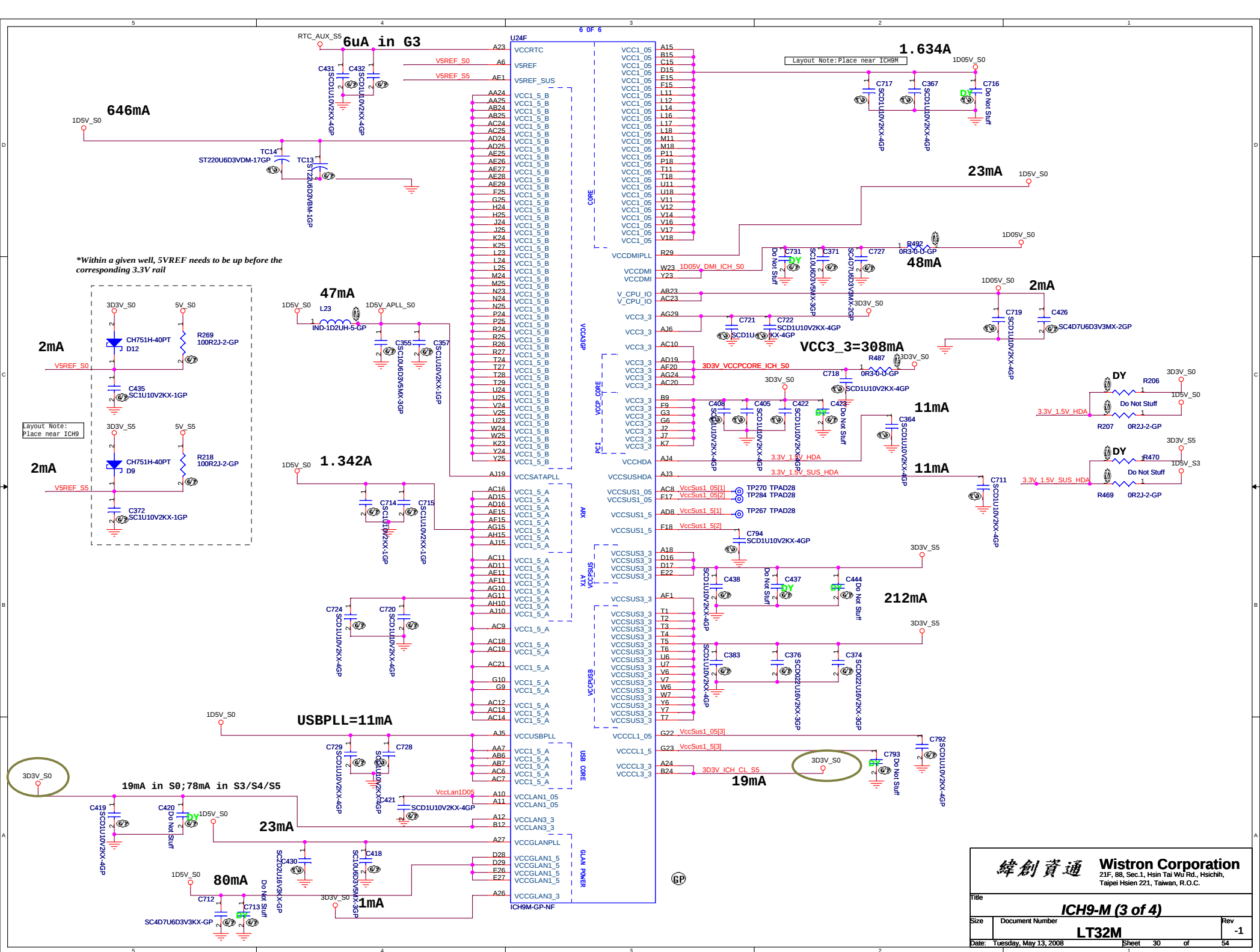
Rev

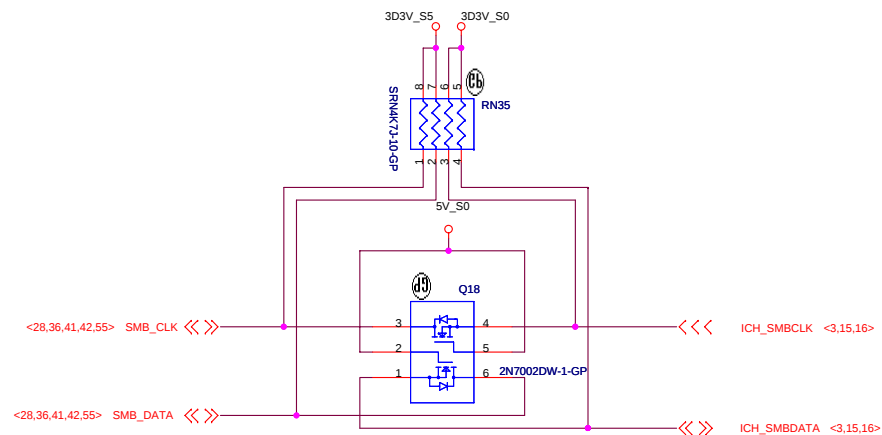
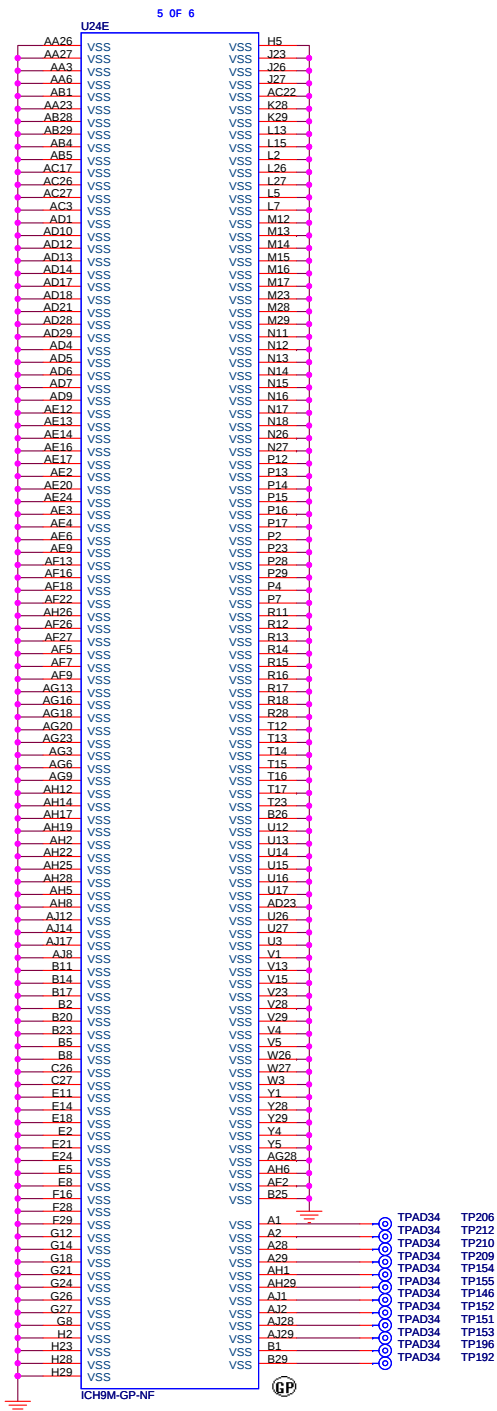
SB

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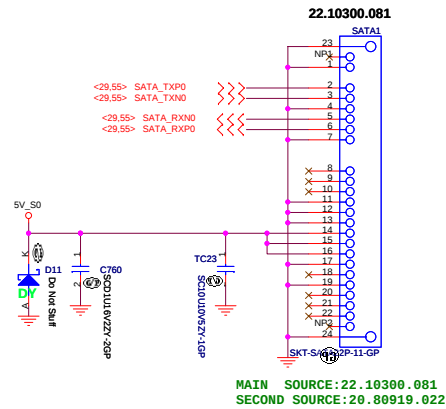




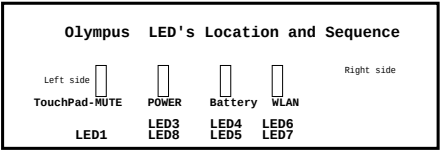
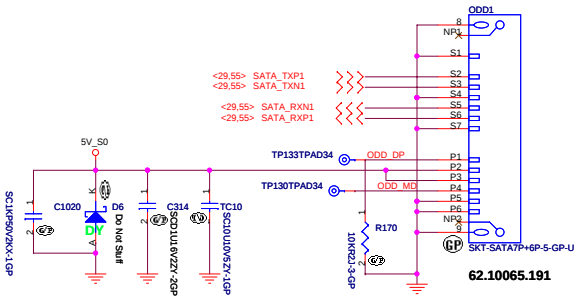
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

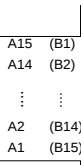
SATA HD Connector



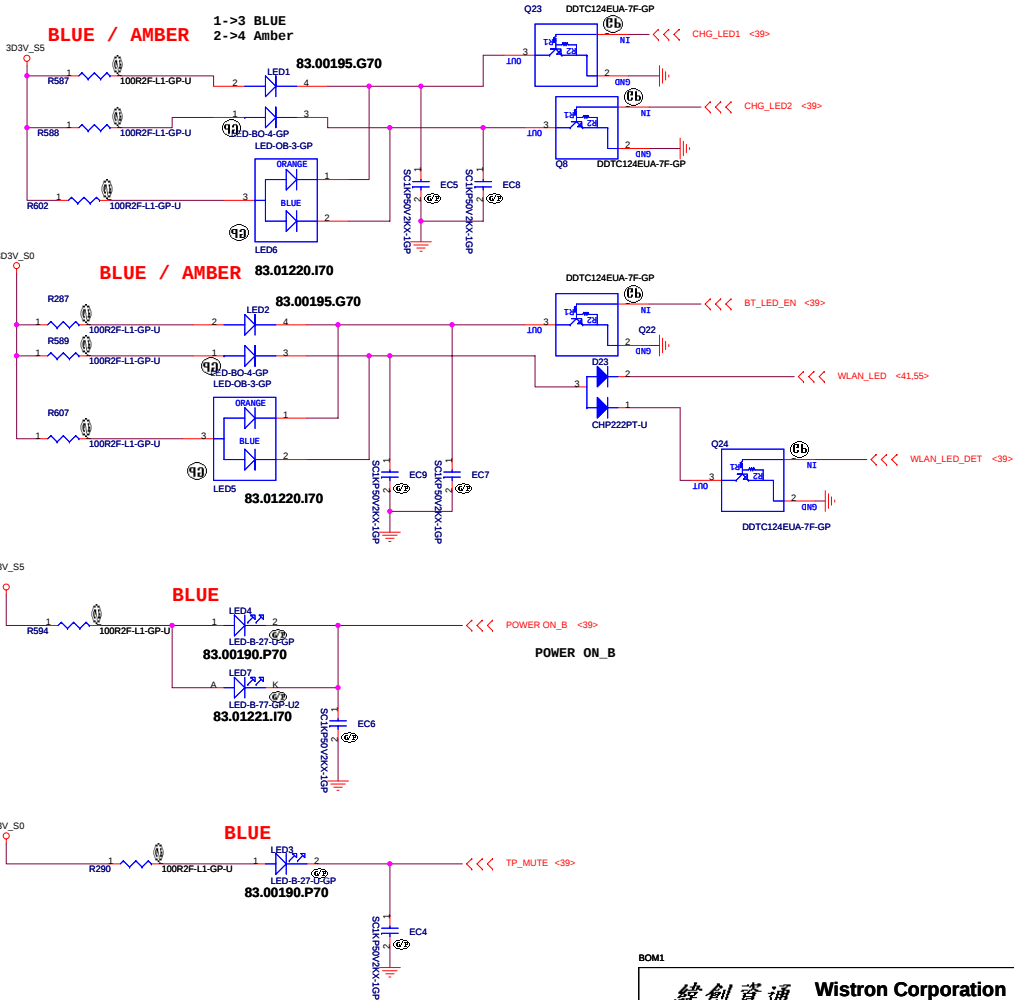
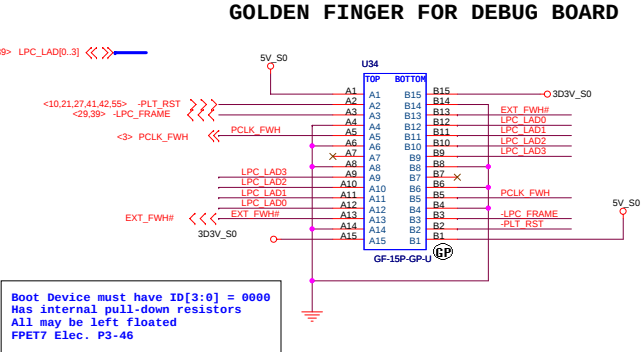
ODD Connector

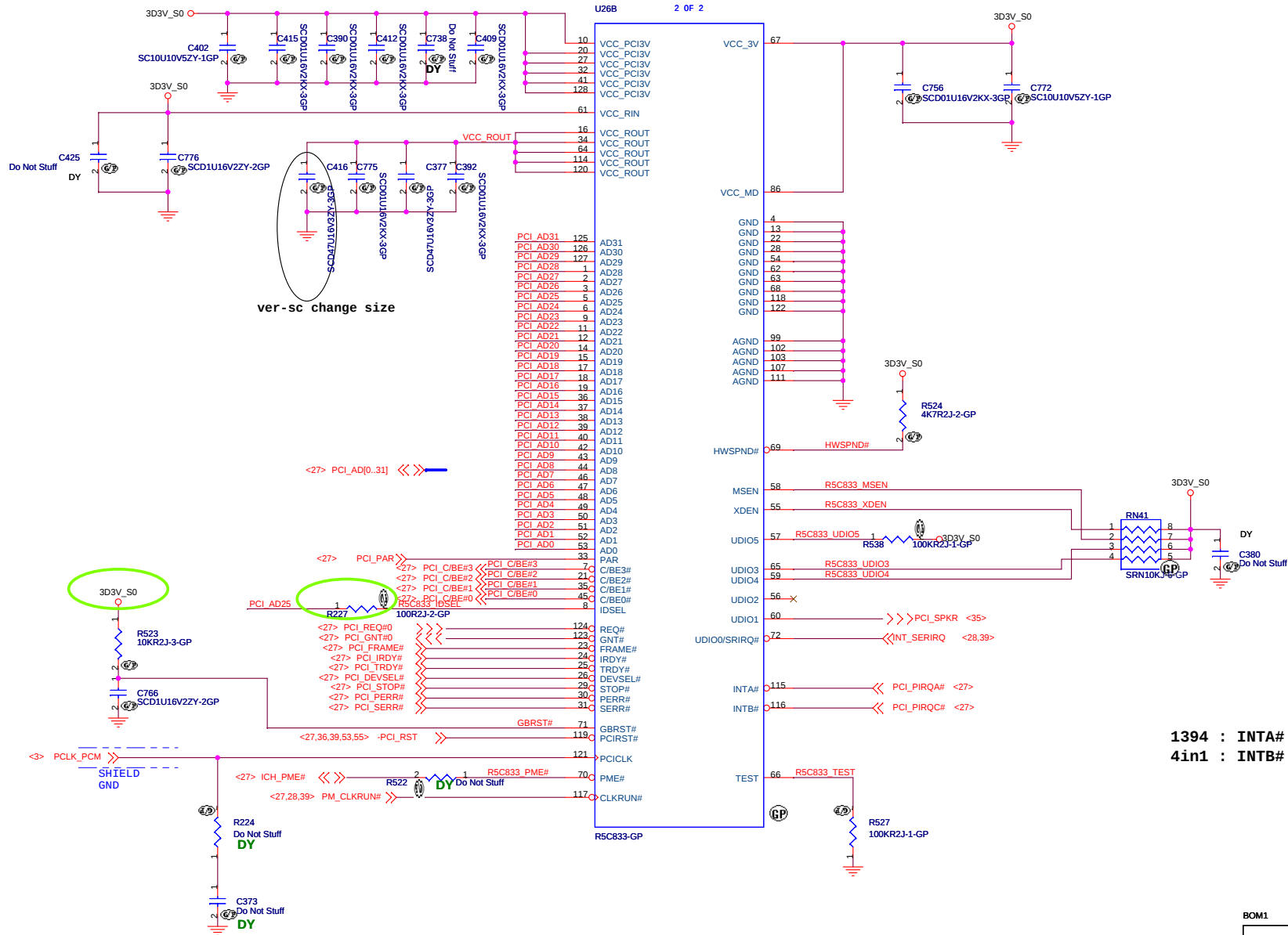


TOP VIEW

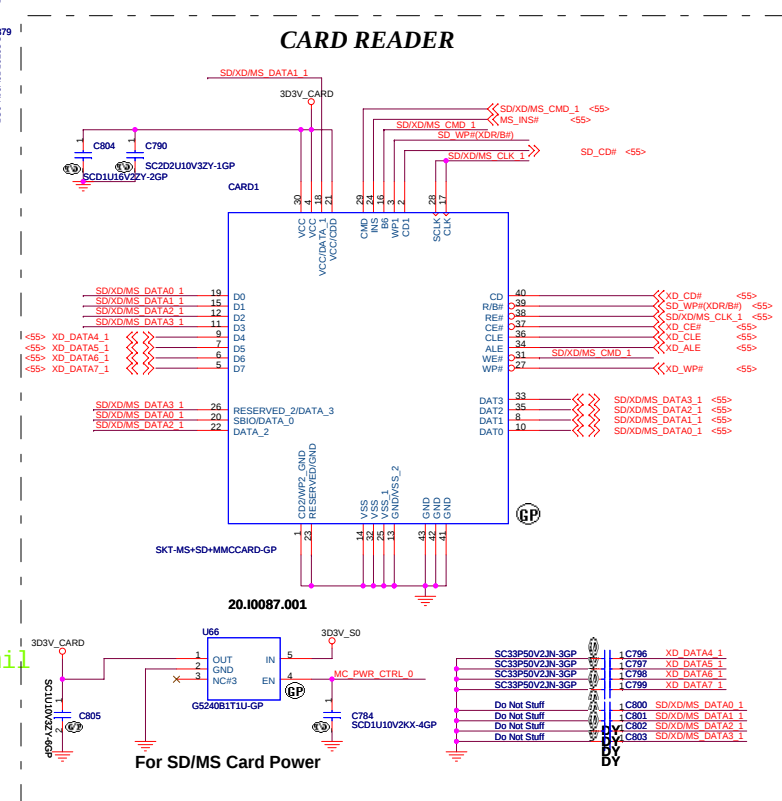


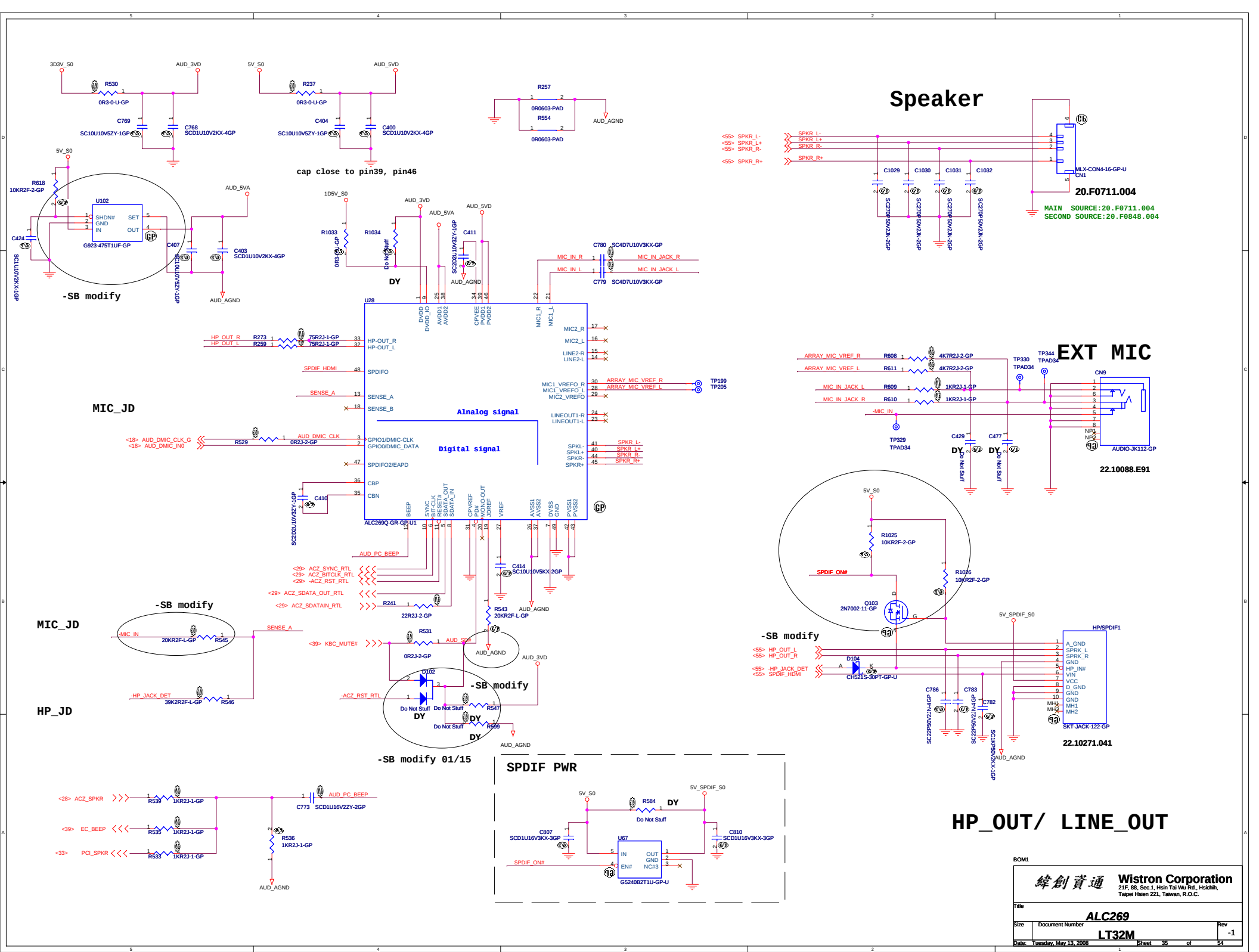
(BOTTOM VIEW)

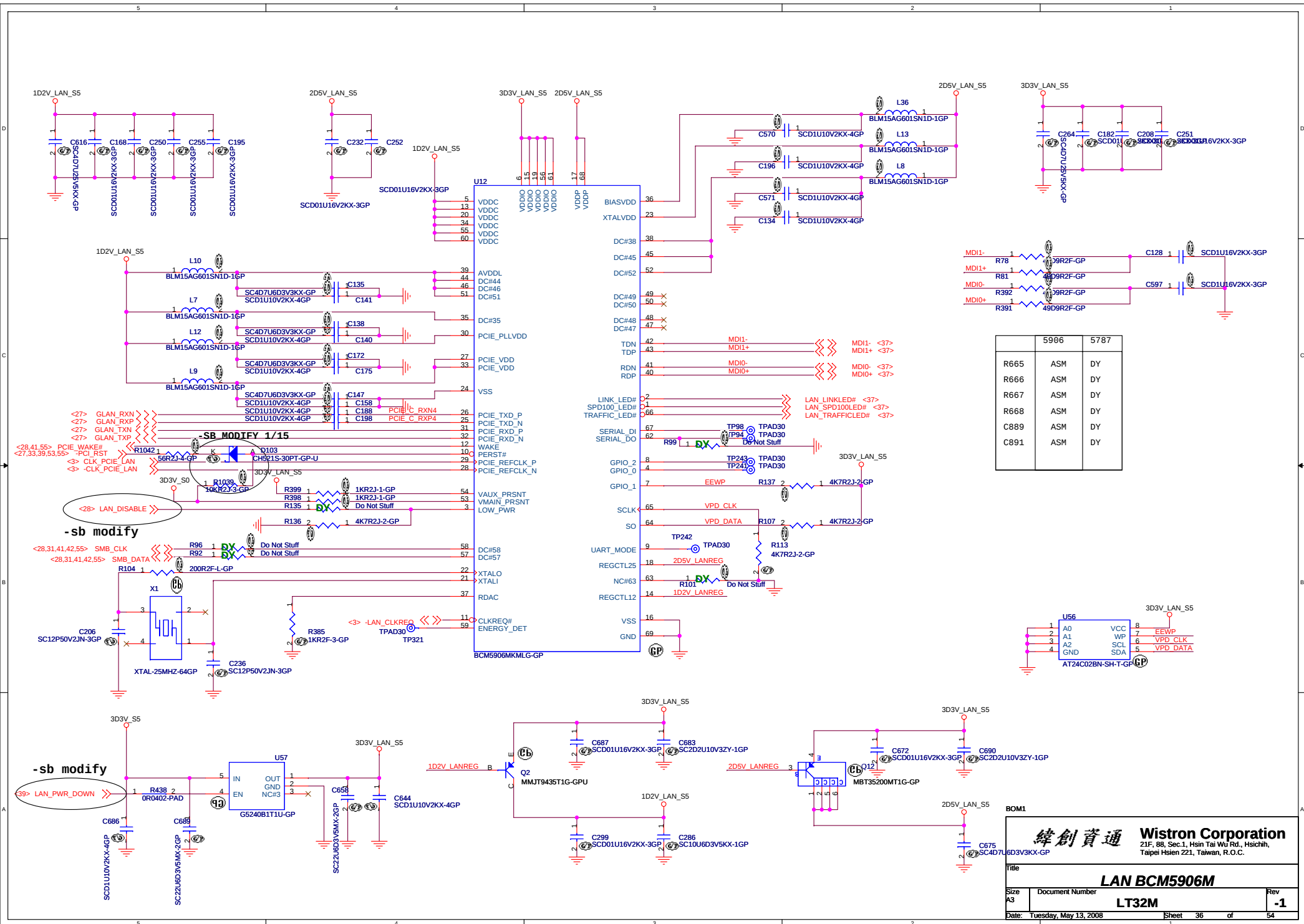




BOM1







	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

BOM1

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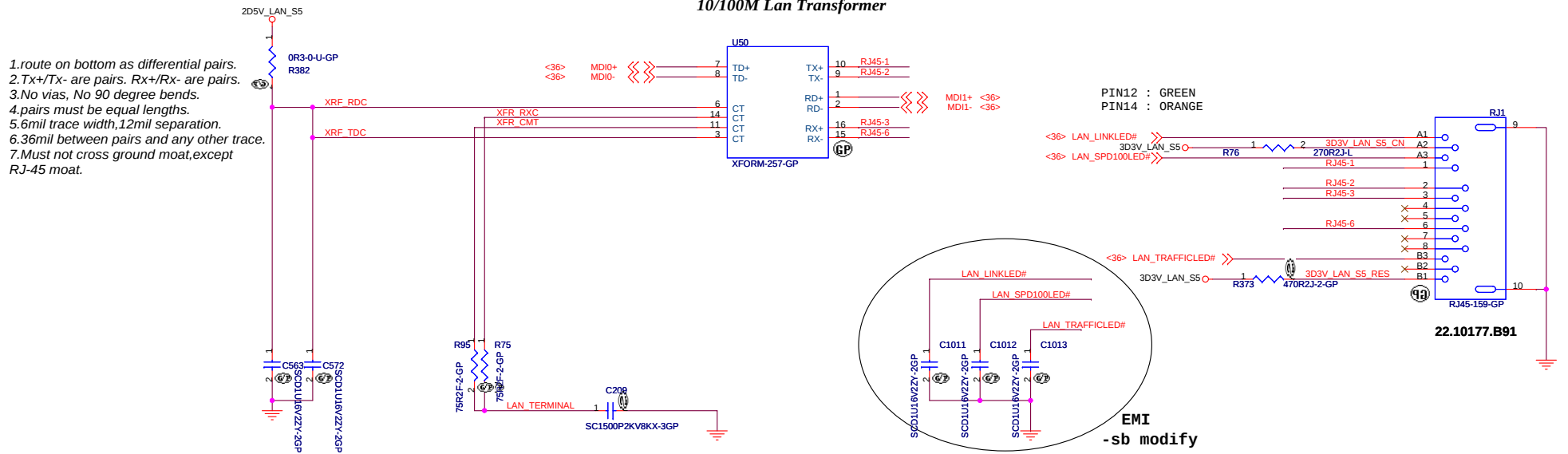
File **LAN BCM5906M**

Size **Document Number** **Rev**

A3 **LT32M** **-1**

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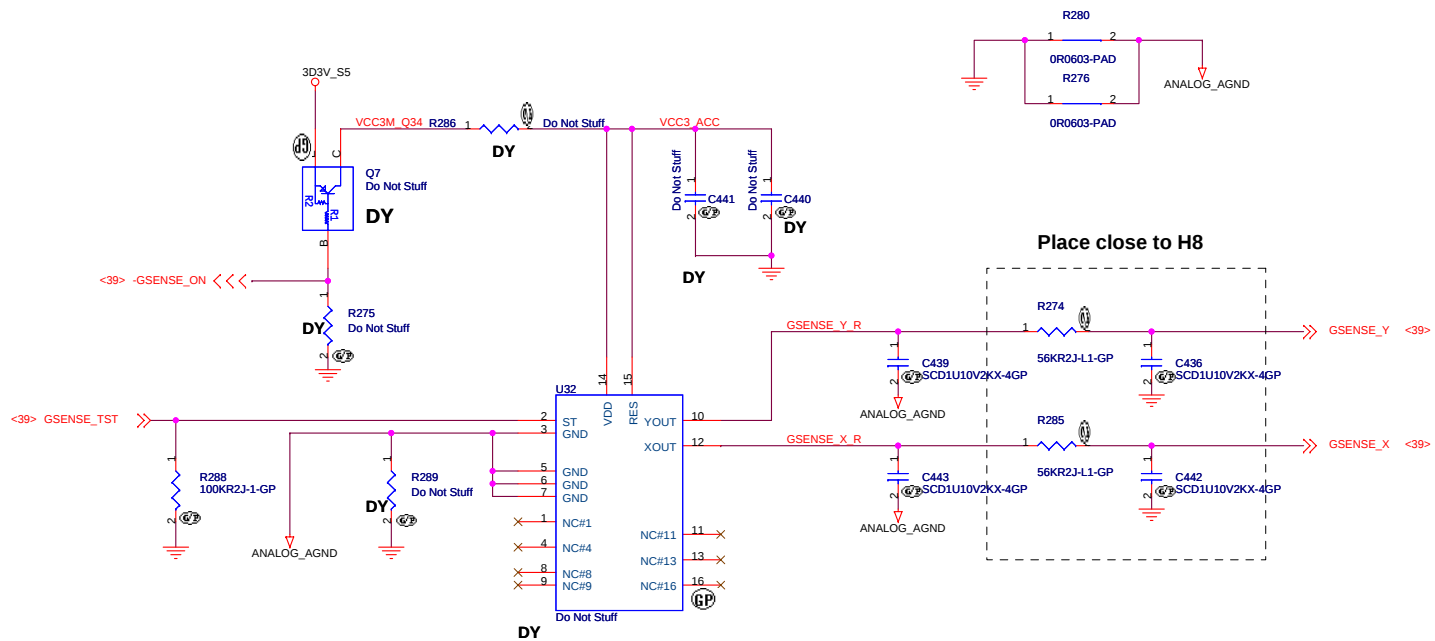
10/100M Lan Transformer



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN connector/NEW CARD/SIM			
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Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil
for three Output traces

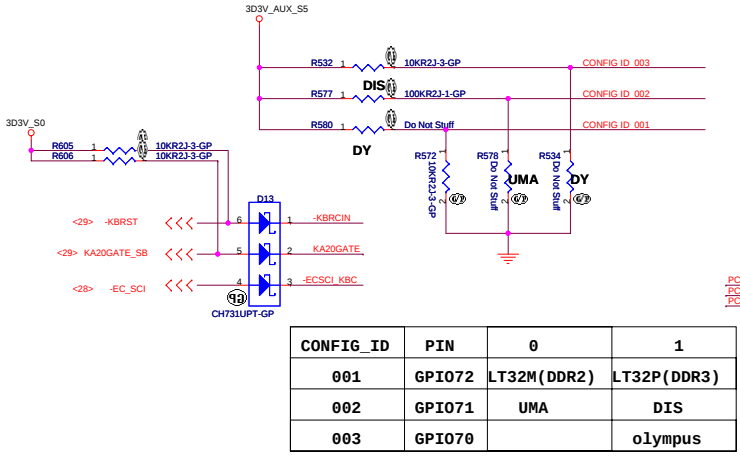
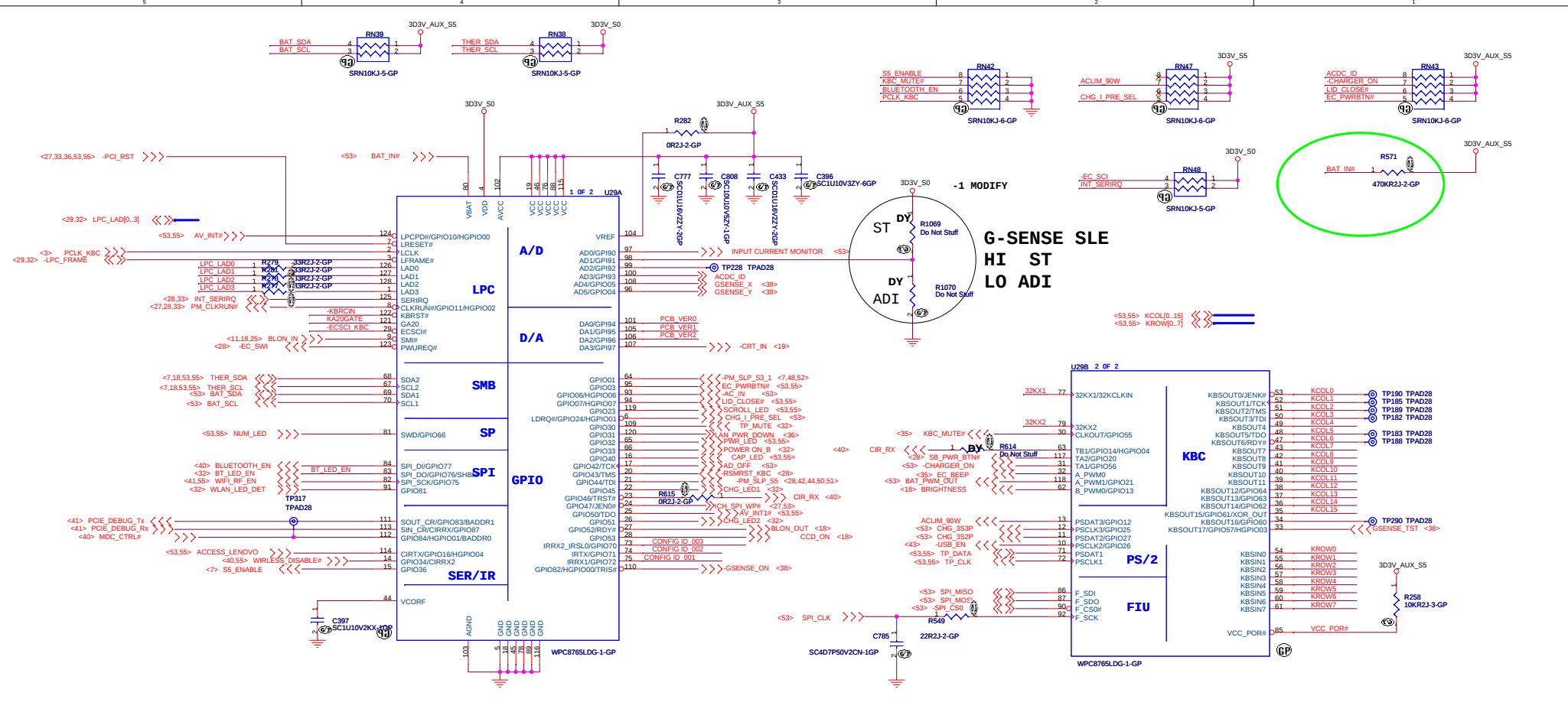
	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

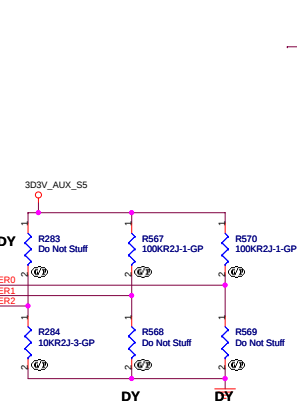
- (1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.
- (2) Avoid routing under DCDC switching area.

BOM1

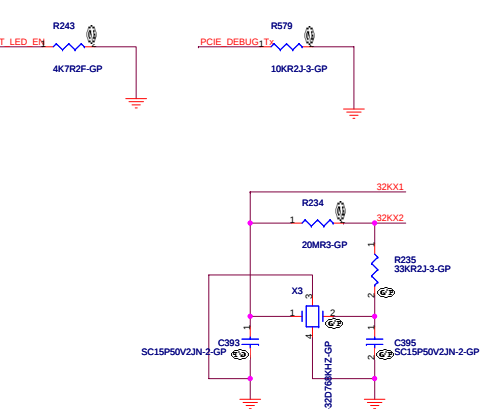
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		G-SENSOR	
Size A3	Document Number	LT32M	Rev -1
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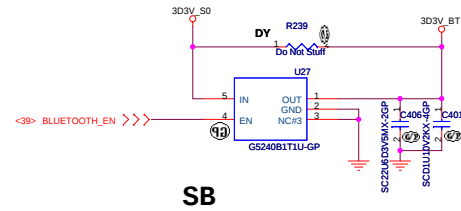


CONFIG_ID	PIN	0	1
001	GPI072	LT32M(DDR2)	LT32P(DDR3)
002	GPI071	UMA	DIS
003	GPI070		olympus

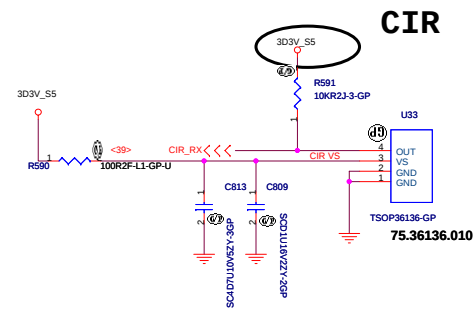
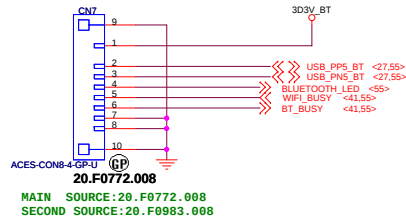


PID_LAB1 = 000b ; Lab1
 PID_LAB2 = 001b ; Lab2
 PID_ENG = 010b ; ENG
 PID_PD = 011b ; PD

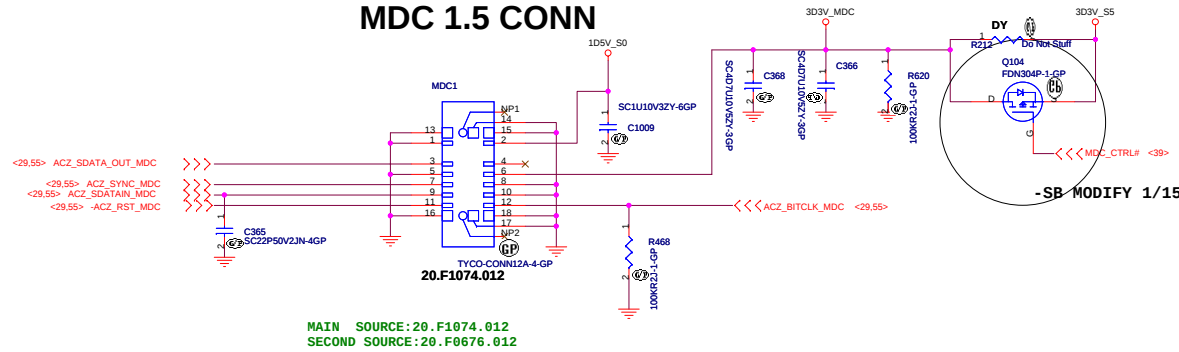




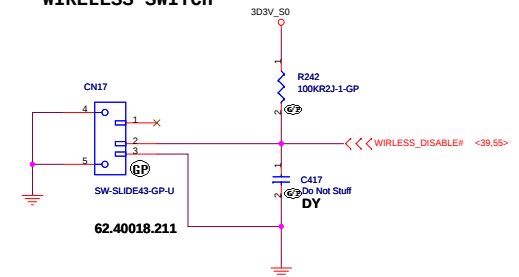
BT CONNECTOR



MDC 1.5 CONN



WIRELESS SWITCH



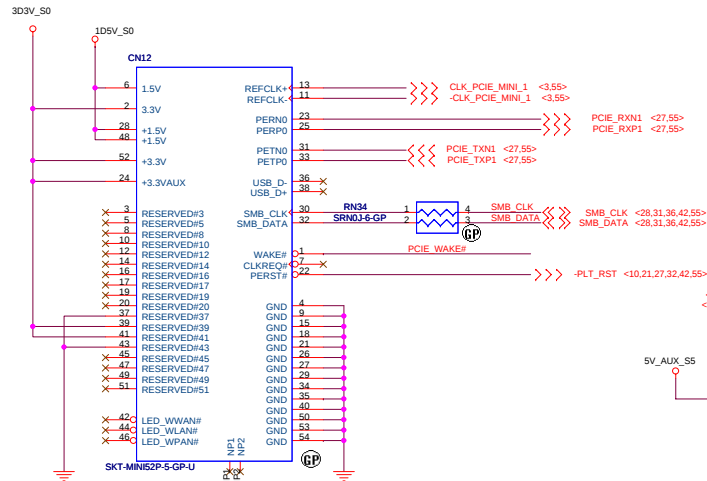
BOML

Mini PCI-E Connector

Only port-1 support USB

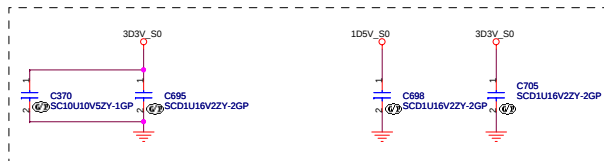
For Robson

Port-1 High



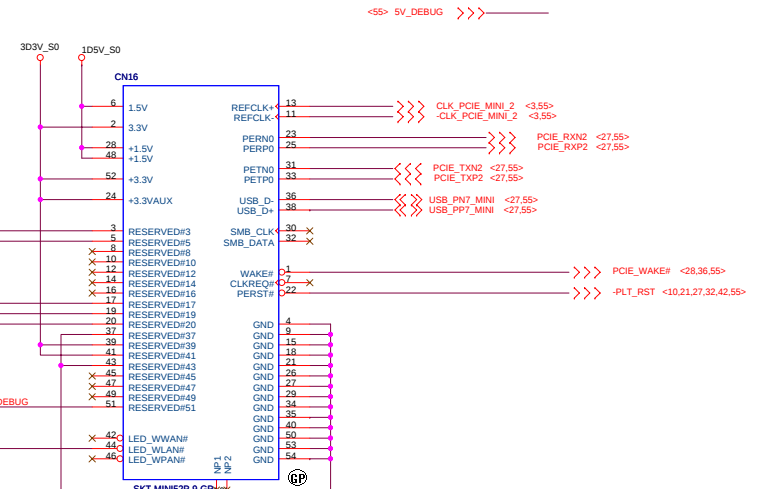
20.F0832.052

MAIN SOURCE: 20.F0832.052
SECOND SOURCE: 20.F1107.052



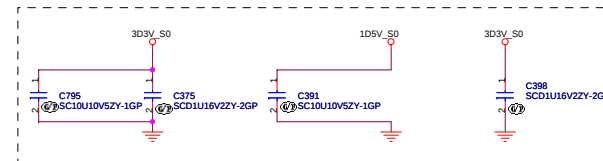
Mini PCI-E Connector

Port-2 low



62.10043.411

MAIN SOURCE: 62.10043.411
SECOND SOURCE: 20.F1084.052



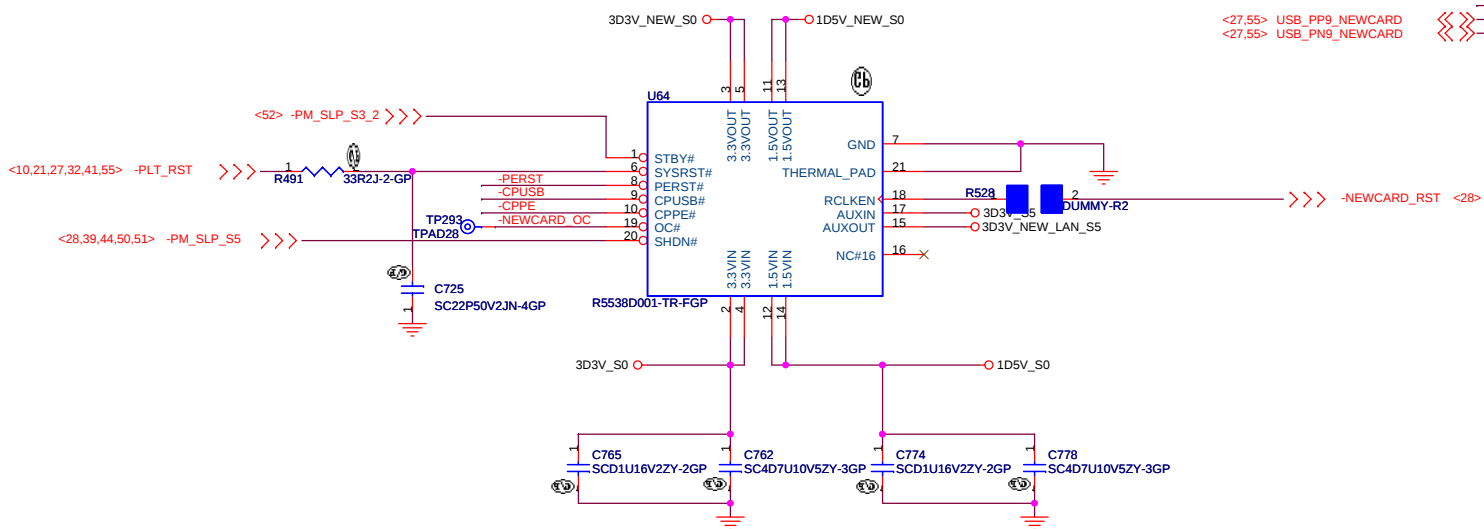
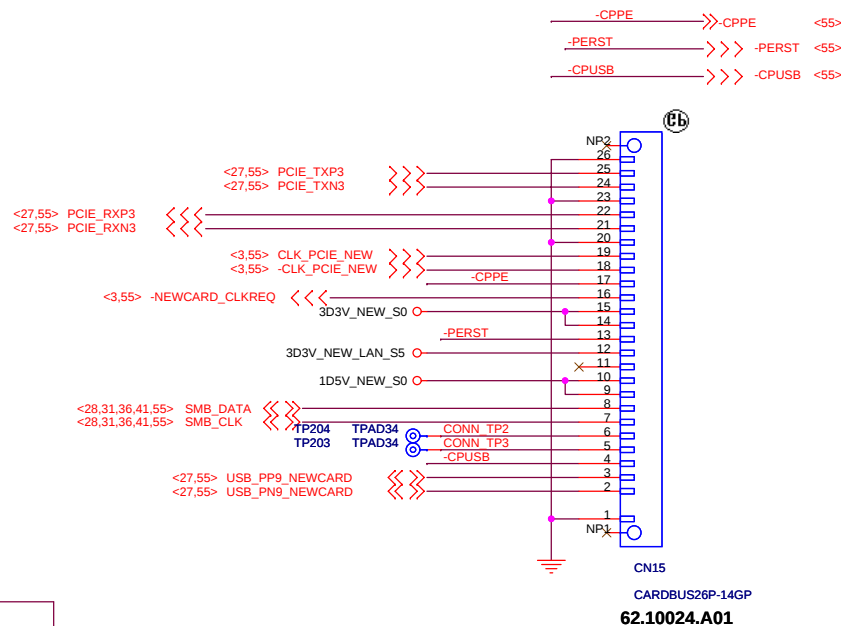
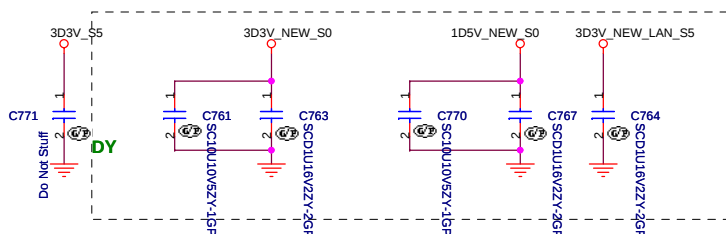
BOCM1

NEWCARD Connector

For Newcard socket

Place them Near to Chip

Place them Near to Connector



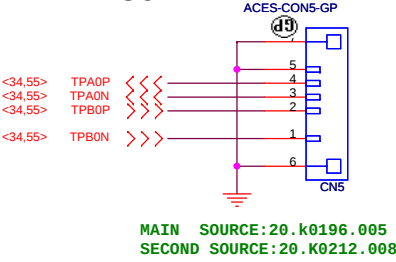
BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

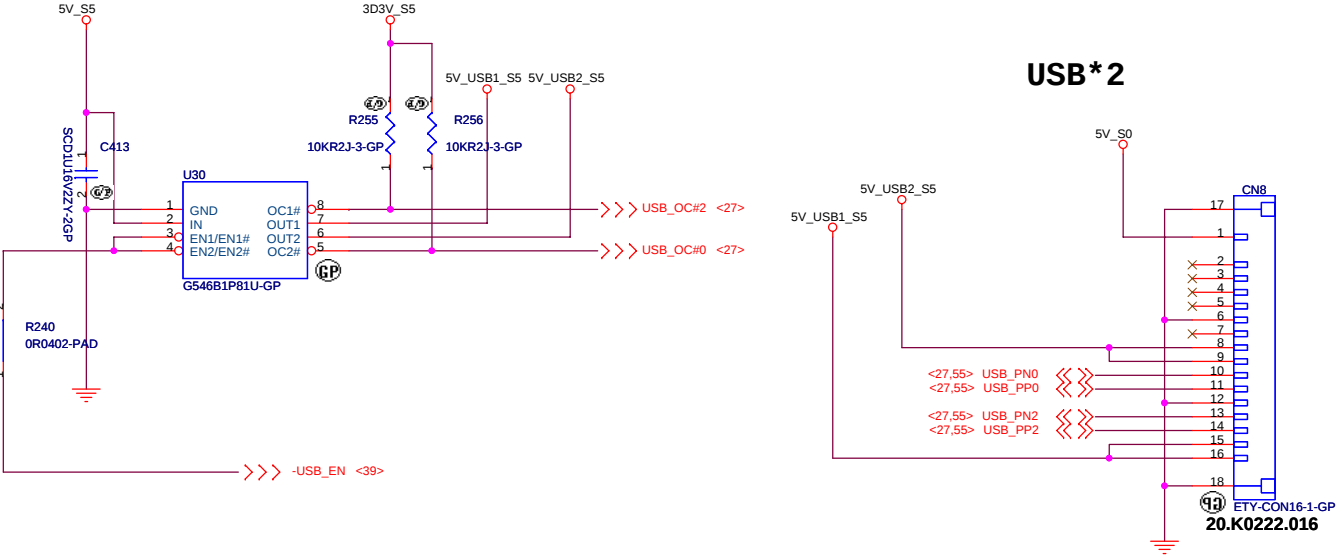
Title			
Module NewCard			
Size	Document Number		Rev
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Low -End USB BOARD

1394

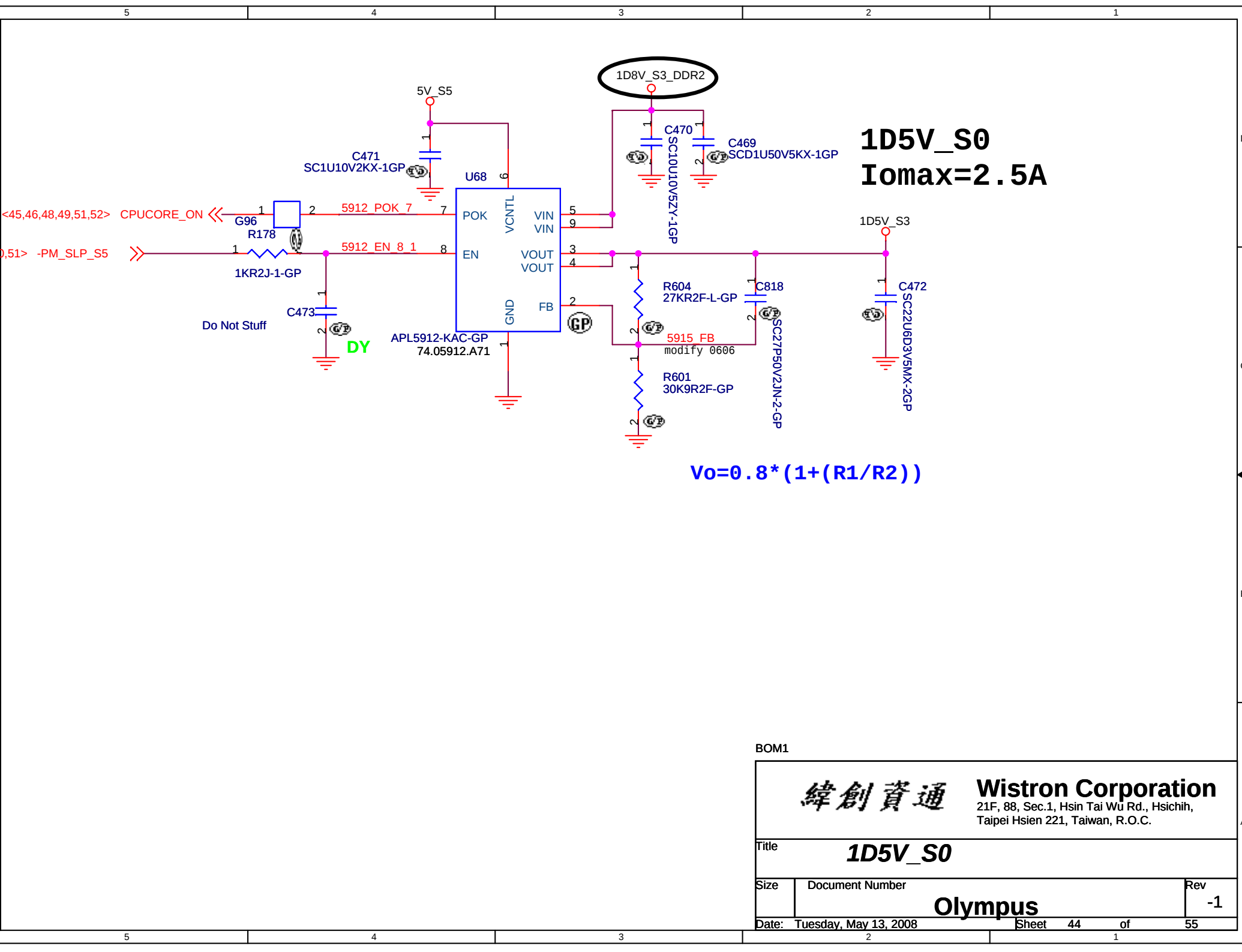


USB*2



BOM1			
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Title			
USB I/O & 1394 CNN			
Size	Document Number		Rev
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D
C
B
A



BOM1

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

1D5V_S0

Size

Document Number

Rev

Olympus

-1

Date: Tuesday, May 13, 2008

Sheet

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55

-SC MODIFY 1/15

<10.28> PM_DPRSLPVR
<4.10.29> -DPRSTP
<10.28> -VGAET_PWRG

-1 MODIFY

-1 MODIFY

-1 MODIFY

-1 MODIFY

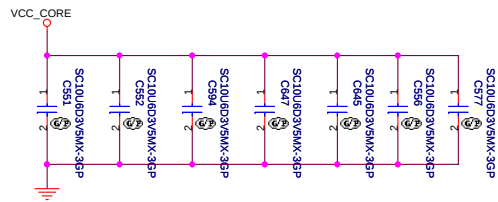
sc-modify

Iomax: 38A

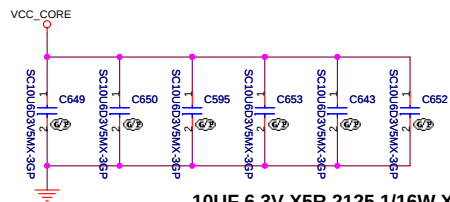
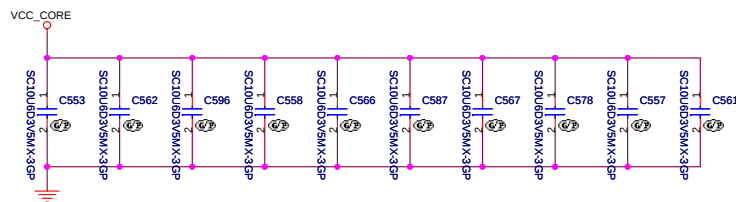
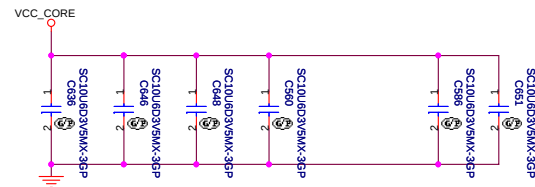
CPU noise

Place close to 1st phase choke

Place close to 1st Choke



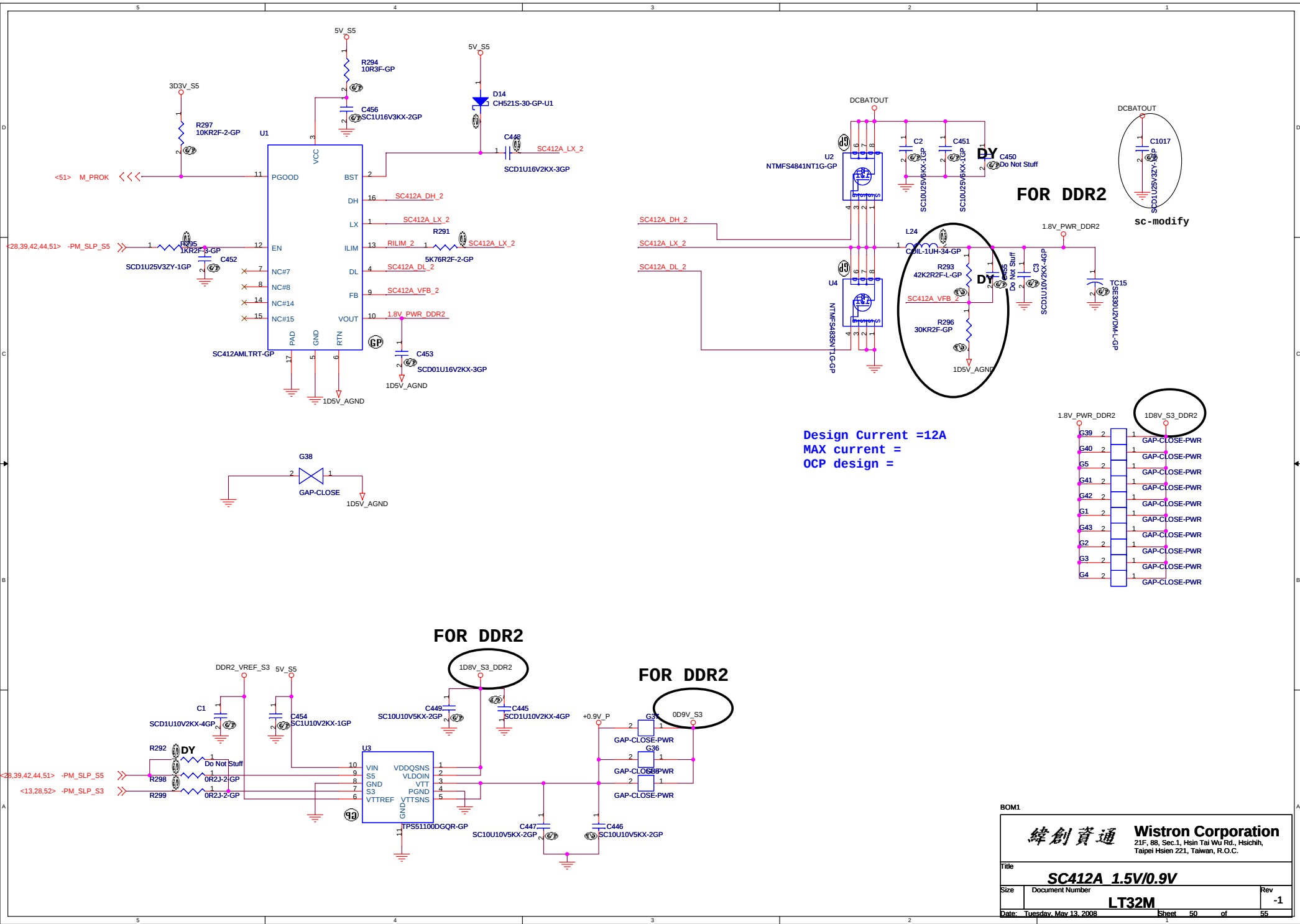
10UF 6.3V X5R 2125 1/16W X16 PCS



10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

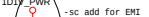
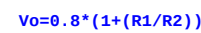
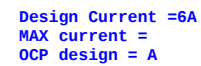
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
file			
VCCCPUCORE DECOUPLING			
Size	Document Number		Rev
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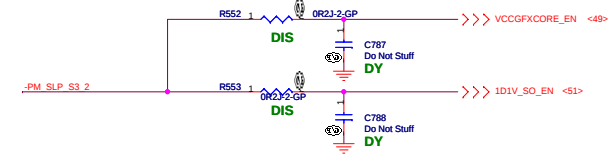
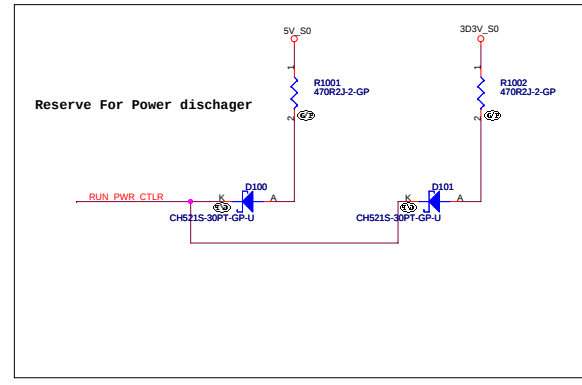
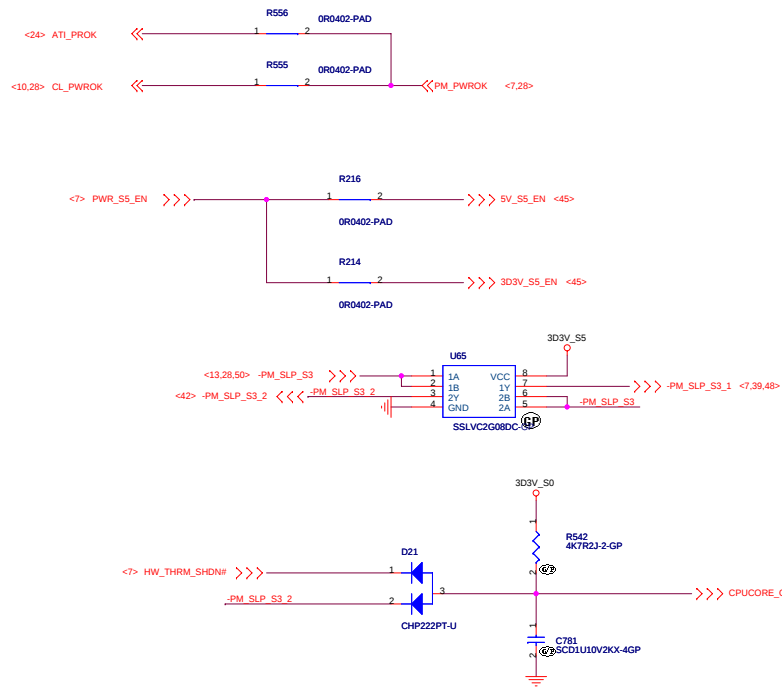


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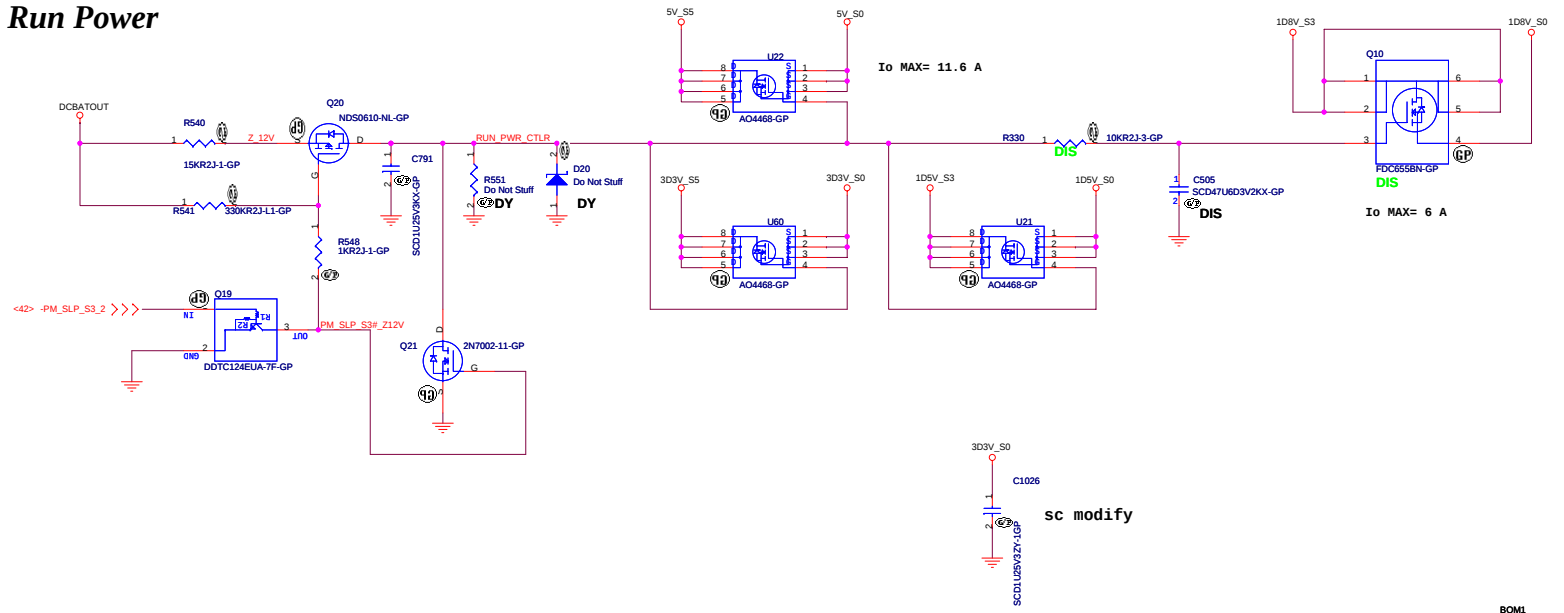
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

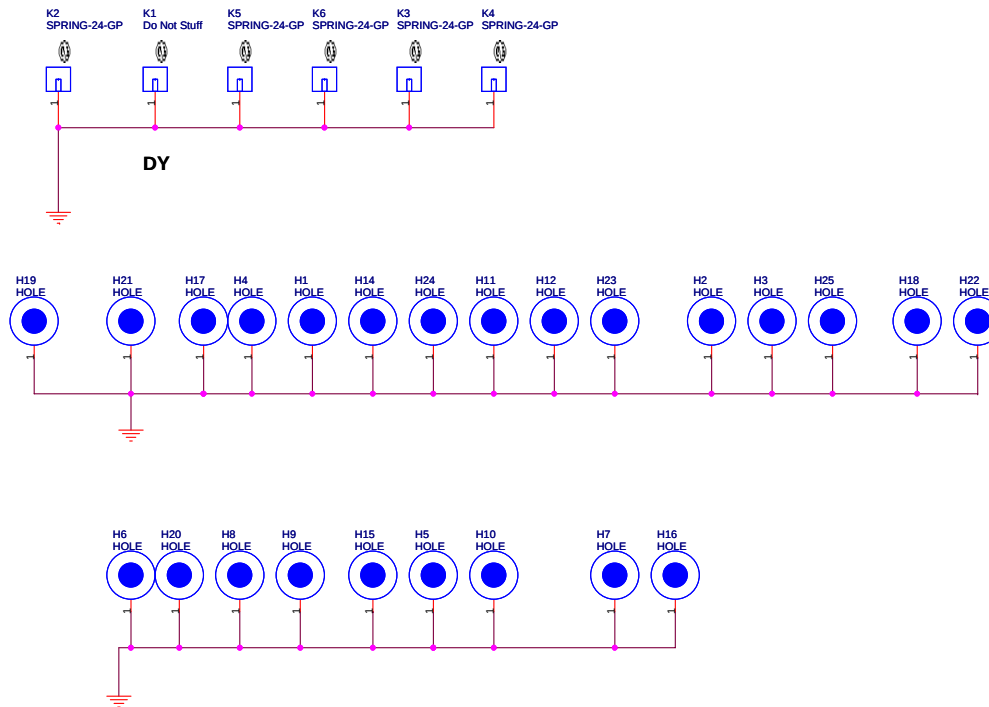
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Size	Document Number	LT32M	
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Run Power





BOM1

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PTH FOR SCREW HOLES					
Title					
Size	Document Number				Rev
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